UNIT IV

FIELD EFFECT TRANSISTOR

Junction field effect transistor (construction, principle of operation, symbol)

Pinch-off voltage

Volt-ampere characteristics

MOSFET (construction, principle of operation, symbol)

Characteristics in enhancement and depletion modes

Small signal model of JFET & MOSFET

FIELD EFFECT TRANSISTOR (FET):

The Field Effect Transistor abbreviated as FET is an another semi conductor device like a BJT which can be used as an amplifier or switch.

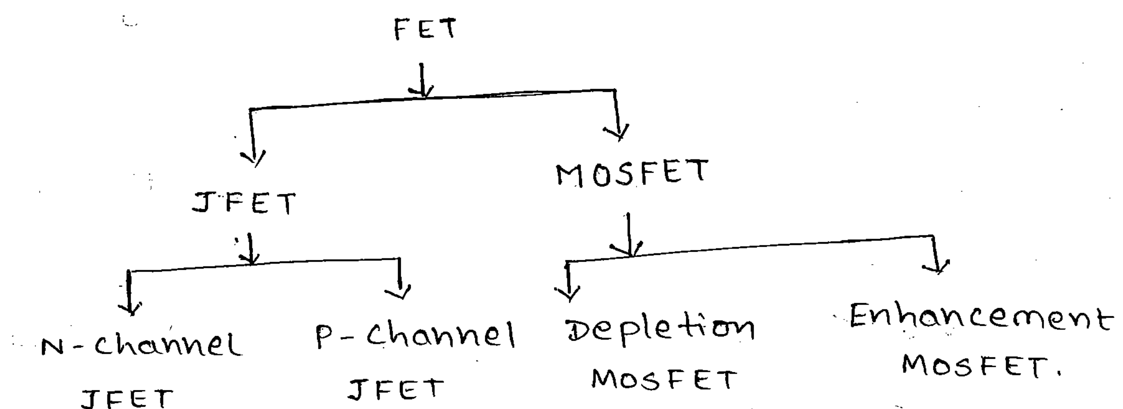
Like BJT, FET is also a three terminal device, however the principle of operation of FET is completely different from that of BJT.

The name Field Effect is derived from the fact that the flow of current through the conducting region is controlled by an electric field.

Types of FET :-

Based on the construction, the FET can be classified in to two types

1. Junction Field Effect Transistor (JFET)
2. Metal oxide semiconductor Field Effect Transistor (MOSFET) (or) Insulated Gate FET (IGFET) (or) Metal oxide silicon transistor (MOST)



Features of FET :

→ FET is a voltage controlled device because output current is controlled by varying the input voltage

→ FET is a unipolar device because the current conduction is only by Majority charge carriers.

→ The three terminals of FET are named as Drain (D), Source (S) and Gate (G). out of these terminals gate terminal acts as controlling element.

→ FET is more temperature stable as compared to BJT.

→ FET has very high input Impedance. Typically in the range of several Mega ohms. FET has higher input impedance than BJT, so FET is preferred in Amplifiers where high input impedance is required

→ Fet's require less space than that of BJT hence they are prefered in Integrated Circuits.

Junction Field Effect Transistor (JFET) :-

Depending upon the Majority carriers JFET has been classified in to two types.

1) N-channel JFET with electrons as the majority charge carriers

2) P-channel JFET with holes as the majority charge carriers.

Construction and Symbol of N-channel JFET :

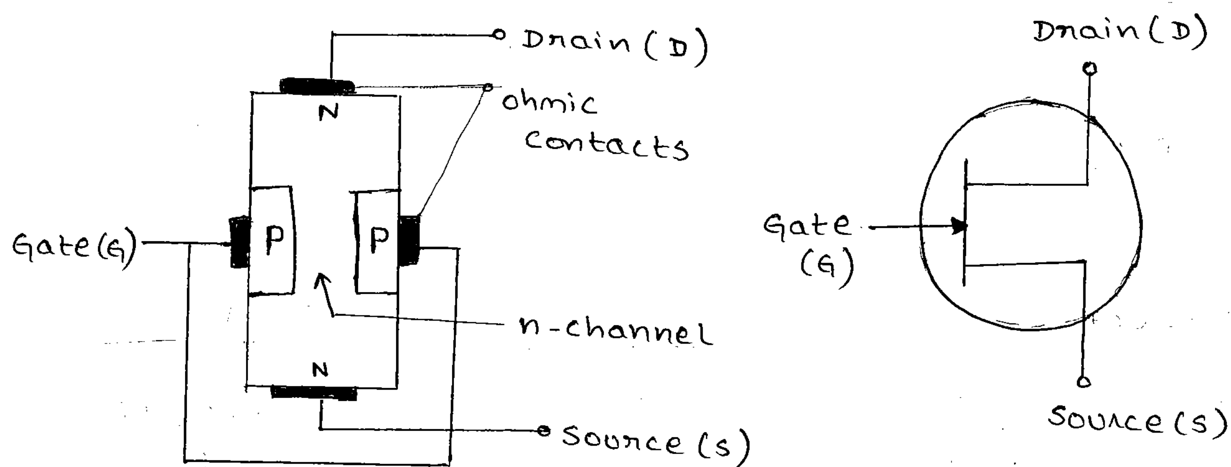


Fig: structure and symbol for n-channel JFET.

It consists of a N-type bar which is made of silicon. ohmic contacts (terminals) made at the two ends of the bar, are called source and drain.

Source (S) : This terminal is connected to the negative terminal of the battery. Electrons which are the majority carriers in the N-type bar enter the bar through this terminal.

Drain (D) : This terminal is connected to the positive terminal of the battery. The majority carriers leave the bar through this terminal.

Gate (G) : Heavily doped P-type silicon is diffused on both sides of the N-type silicon bar by which PN junctions are formed. These layers are joined together and called Gate (G).

Channel: The thin region between the two P-Gates is called the channel. Since this channel is in the n-type bar, the FET is known as n-channel JFET.

Construction (structure) and symbol of P-channel JFET:

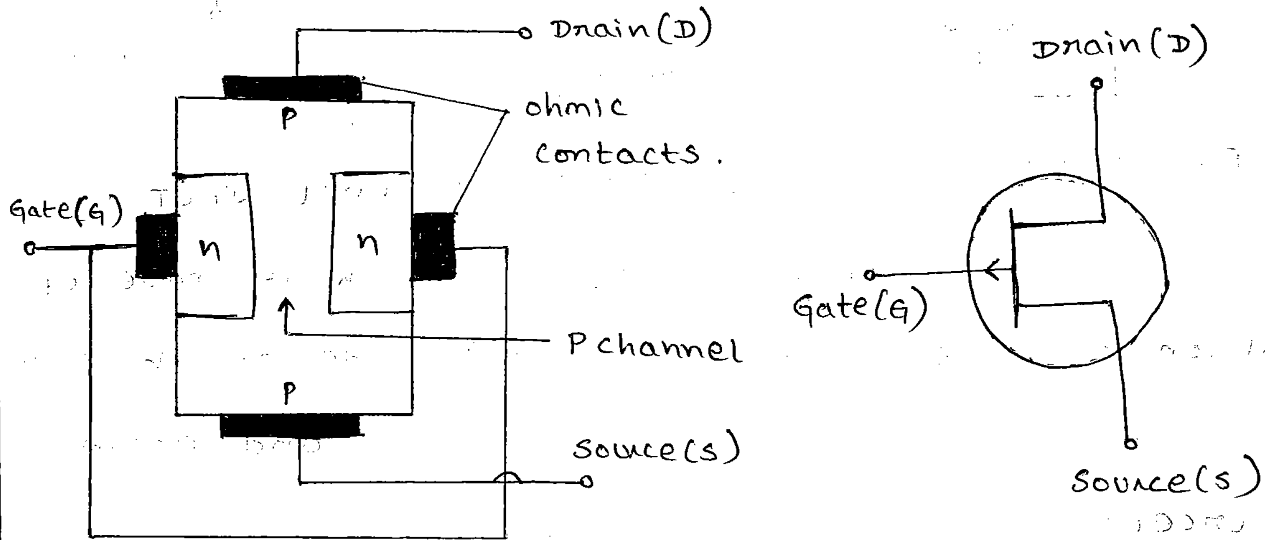
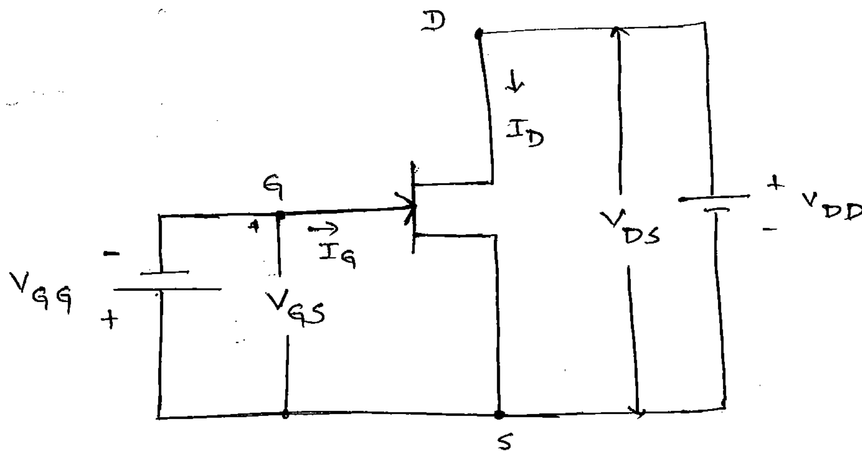


Fig: Structure and symbol for P-channel JFET

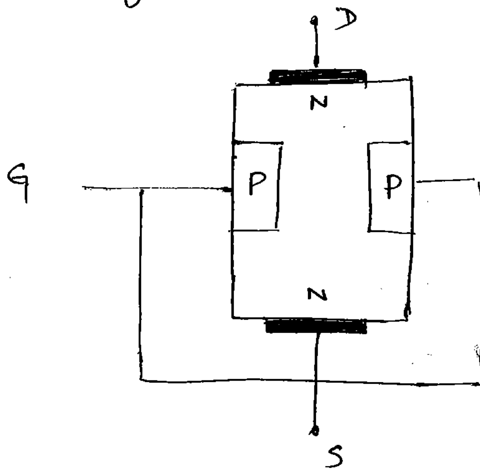
The device is made of P type bar with two n-type gates as shown in figure. The principle of working of P-channel JFET and n-channel JFET is similar. The only difference is that, in n-channel JFET the current is carried by electrons while in P-channel JFET, it is carried by holes.

Operation of N-channel JFET {Static characteristics of JFET}

i) when V_{GS} zero and The circuit symbol for N-channel JFET is shown in figure below.



1) when $V_{GS} = 0$ and $V_{DS} = 0$:- when no voltage is applied between drain and source, and gate and source, the thickness of the depletion regions round the PN junctions is uniform as shown in figure below.



2) when $V_{DS} = 0$ and V_{GS} is decreased from zero :-

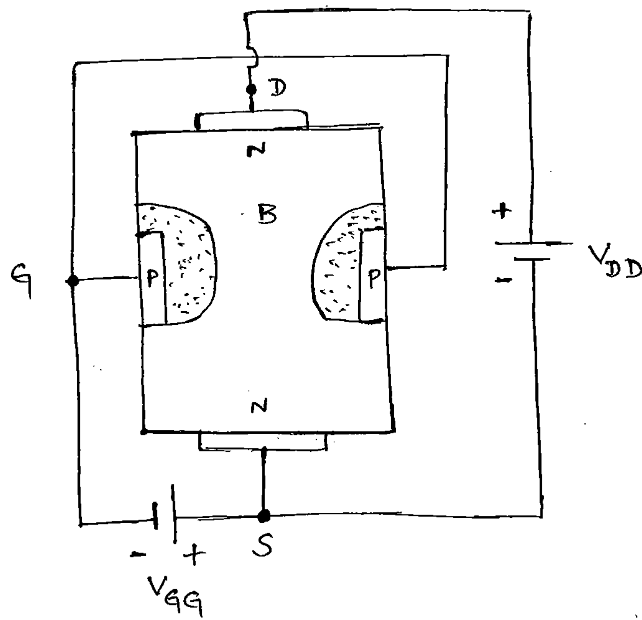
In this case, the PN junctions are reverse biased and hence the thickness of the depletion region increases

As V_{GS} is decreased from zero, the reverse bias voltage across the PN junction is increased and hence, the thickness of the depletion region in the channel, until the two depletion regions make contact with each other. In this condition the channel is said to be cut-off. The value of V_{GS} which is required to cut-off the channel is called the cut-off voltage.

3) <u>when $V_{GS} = 0$ and V_{DS} is increased from zero</u> :-

Drain is positive with respect to the source with $V_{GS} = 0$. Now the majority carriers ie electrons flow through the N-channel from source to drain. Therefore the conventional current I_D flows from Drain to Source. The magnitude of current will depend upon the ~~following factor~~ so many factors. Thus the channel acts as a resistor.

Because of the resistance of the channel and the applied voltage V_{DS}, there is a gradual increase of positive potential along the channel from source to drain. Thus the reverse voltage across the PN junction increases and hence the thickness of the depletion regions also increases. Therefore the channel is wedge shaped as shown in figure below.



As V_{DS} is increased, the cross sectional area of the channel will be reduced. At a certain value of V_{DS}, the cross sectional area at B becomes minimum. At this voltage, the channel is said to be pinched off and the corresponding V_{DS} is called pinch-off voltage (V_P)

As a result of the decreasing cross section of the channel with the increase of V_{DS}, the following results are obtained.

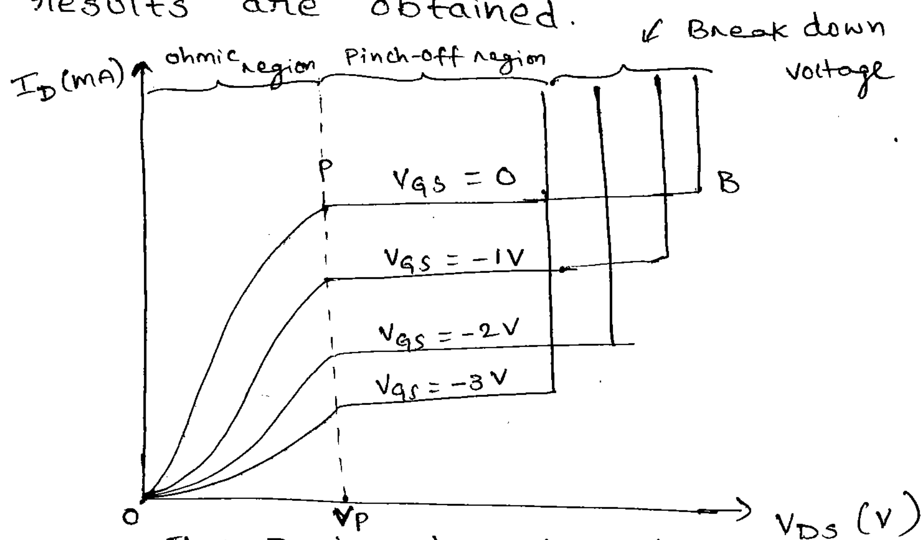


Fig: Drain characteristics.

i) As V_{DS} is increased from zero, I_D increases along OP. The region from $V_{DS} = 0V$ to $V_{DS} = V_P$ is called the ohmic region.

ii) When $V_{DS} = V_P$, I_D becomes maximum. When V_{DS} is increased beyond V_P, the length of the pinch-off region increases. Hence there is no further increase of I_D.

iii) At a certain voltage corresponding to the point B, I_D suddenly increases. This effect is due to the Avalanche multiplication of electrons caused by breaking of covalent bonds of silicon atoms in the depletion region between the gate and drain.

4) When V_{GS} is negative and V_{DS} is increased :-

When the gate is maintained at a negative voltage less than the negative cut-off voltage, the reverse voltage across the junction is further increased. Hence for a negative value of V_{GS}, the curve of I_D versus V_{DS} is shown in figure above.

From the curves it is seen that above the pinch-off voltage, at a constant value of V_{DS}, I_D increases with an increase of V_{GS}. Hence a JFET is suitable for use as a voltage amplifier, similar to a transistor amplifier.

Characteristic parameters of the JFET

In a JFET, the drain current I_D depends upon the drain voltage V_{DS} and the gate voltage V_{GS}. Any one of these variables may be fixed and the relation between the other two are determined. These relations are determined by the three parameters which are defined below.

1) Transconductance (or) Mutual conductance (g_m) :-

It is the slope of the transfer characteristic curves, and is defined by

$$g_m = \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} = \frac{\Delta I_D}{\Delta V_{GS}}, \quad V_{DS} = \text{constant}$$

It is the ratio of a small change in the drain current to the corresponding small change in the gate voltage at a constant drain voltage.
It has the unit of conductance in mho.

2) Drain Resistance (r_d) :- It is the reciprocal of the slope of the drain characteristics and is defined by

$$r_d = \left(\frac{\partial V_{DS}}{\partial I_D}\right)_{V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D}, \quad V_{GS} = \text{constant}$$

It is the ratio of a small change in the drain voltage to the corresponding small change in

the drain current at a constant gate voltage. It has the unit of resistance in ohms.

3) Amplification factor (μ) : It is defined by

$$\mu = -\left(\frac{\partial V_{DS}}{\partial V_{GS}}\right)_{I_D} = \frac{\Delta V_{DS}}{\Delta V_{GS}}, \quad I_D = \text{constant}$$

It is the ratio of a small change in the drain voltage to the corresponding small change in the gate voltage at a constant drain current. Here the negative sign shows that when V_{GS} is increased, V_{DS} must be decreased for I_D to remain constant.

Relationship among FET parameters :-

As I_D depends on V_{DS} and V_{GS}, the functional equation can be expressed as

$$I_D = f(V_{DS}, V_{GS})$$

If the drain voltage is changed by a small amount from V_{DS} to $(V_{DS} + \Delta V_{DS})$ and the gate voltage is changed by a small amount from V_{GS} to $(V_{GS} + \Delta V_{GS})$, then the corresponding small change in I_D may be obtained by applying Taylor's theorem with neglecting higher order terms. Thus a small change ΔI_D is given by

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \Delta V_{DS} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} \Delta V_{GS}$$

dividing both the sides of this equation by ΔV_{GS}, we obtain

$$\frac{\Delta I_D}{\Delta V_{GS}} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)_{I_D} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

If I_D is constant then $\frac{\Delta I_D}{\Delta V_{GS}} = 0$

$$0 = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)_{I_D} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

substituting the values of partial differential co-efficients, we get

$$0 = \left(\frac{1}{r_d}\right)(-\mu) + g_m$$

$$g_m = \frac{\mu}{r_d} \Rightarrow \boxed{\mu = r_d \times g_m}$$

therefore amplification factor (μ) is the product of drain resistance (r_d) and transconductance (g_m)

Problem: when a reverse gate voltage of 12V is applied to JFET, the gate current is 1nA. Determine the resistance between gate and source.

Sol: $V_{GS} = 12\,V$, $I_G = 1 \times 10^{-9}\,A$

therefore gate to source resistance $= \frac{V_{GS}}{I_G} = \frac{12}{10^{-9}} = 12000\,M\Omega$

Problem: when the reverse gate voltage of ~~12 V is applied~~ ~~to~~ of JFET changes from 4 to 3.9 V, the drain current changes from 1.3 to 1.6 mA. Find the value of transconductance.

Sol:

$$\Delta V_{GS} = 4 - 3.9 = 0.1 \text{ V}$$

$$\Delta I_D = 1.6 - 1.3 = 0.3 \text{ mA}$$

$$\therefore g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.3 \times 10^{-3}}{0.1} = 3 \text{ m mhos}.$$

Expression for saturation drain current (or) Transfer characteristics of JFET.

For the transfer characteristics V_{DS} is maintained constant at a suitable value greater than the pinch-off voltage V_P.

The gate voltage V_{GS} is decreased from zero till I_D is reduced to zero.

The transfer characteristics I_D versus V_{GS} is shown in figure below.

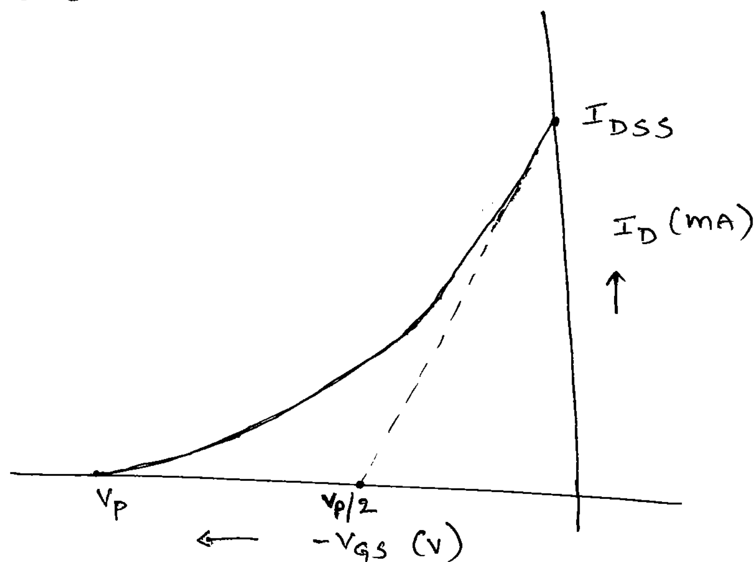


Fig: Transfer characteristics of JFET

The shape of the transfer characteristic is very nearly a parabola. It is found that the characteristic is approximately represented by the parabola.

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \longrightarrow ①$$

where I_{DS} = saturation drain current

I_{DSS} = the value of I_{DS} when $V_{GS} = 0$

V_P = Pinch - off voltage

differentiating eq ① with respect to V_{GS}, we can obtain expression for g_m

$$\frac{\partial I_{DS}}{\partial V_{GS}} = I_{DSS} \times 2\left(1 - \frac{V_{GS}}{V_P}\right)\left(\frac{-1}{V_P}\right)$$

we know that $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$, V_{DS} = constant

$$\therefore \quad g_m = \frac{-2 I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) \longrightarrow ②$$

From Eq ① $\quad 1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_{DS}}{I_{DSS}}}$

Substituting this in eq ②

$$g_m = \frac{-2\sqrt{I_{DS} \, I_{DSS}}}{V_P} \longrightarrow ③$$

suppose when $V_{GS} = 0$, $g_m = g_{mo}$

then from Eq (2) $g_{mo} = \frac{-2 I_{DSS}}{V_p}$ → (4)

therefore from Eq (2) and Eq (4)

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_p}\right)$$

slope of the Transfer characteristic at I_{DSS} :-

From Eq (3) we have

$$g_m = \frac{-2\sqrt{I_{DS}\ I_{DSS}}}{V_p}$$ or

$$\frac{\partial I_{DS}}{\partial V_{GS}} = \frac{-2\sqrt{I_{DS}\ I_{DSS}}}{V_p}$$

substituting $I_{DS} = I_{DSS}$

$$\frac{\partial I_{DS}}{\partial V_{GS}} = \frac{-2 I_{DSS}}{V_p} = \frac{I_{DSS}}{\frac{-V_p}{2}}$$

this equation shows that the tangent to the curve at $I_{DS} = I_{DSS}$, $V_{GS} = 0$, will have an intercept at $\frac{-V_p}{2}$ on the axis of V_{GS} as shown in figure. therefore the value of V_p can be found by drawing the tangent at $I_{DS} = I_{DSS}$, $V_{GS} = 0$

The Gate source cut-off voltage $V_{GS(off)}$ on the transfer characteristic is equal to the pinch-off voltage V_p, on the drain characteristics ie $V_p = |V_{GS(off)}|$

therefore $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$.

Problem: A FET has a drain current of 4mA. If I_{DSS} = 8mA and $V_{GS(off)} = -6V$. Find the values of V_{GS} and V_P.

Solution:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$4m = 8m\left[1 - \frac{V_{GS}}{-6}\right]^2$$

$$\frac{1}{2} = \left(1 + \frac{V_{GS}}{6}\right)^2 \Rightarrow V_{GS} = -1.76\ V$$

$$V_P = |V_{GS(off)}| = 6V.$$

Problem:- An N-channel JFET has I_{DSS} = 8mA. and $V_P = -5V$. Determine the minimum value of V_{DS} for pinch-off region and the drain current I_{DS}, for $V_{GS} = -2V$ in the pinch-off region.

Solution: The minimum value of V_{DS} for pinch-off to occur for $V_{GS} = -2V$ is

$$V_{DS(min)} = V_{GS} - V_P = -2 - (-5) = 3V$$

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_{DS} = 8\times10^{-3}\left[1 - \left(\frac{-2}{-5}\right)\right]^2 = 2.88mA.$$

Comparison of JFET and BJT

1. FET operation depends only on the flow of majority carriers. That's why they are called unipolar devices. BJT operation depends on both minority and majority charge carriers. So BJT is called Bipolar device.

2. As the FET has no junctions and the conduction is through an N-type or P-type semiconductor material. FET is less noisy than BJT.

3. As the input circuit of FET is reverse biased, FET exhibits a much higher input impedance and lower output impedance. So FET can act as excellent buffer amplifier But the BJT has low output impedance because its input circuit is forward biased.

4. FET is a voltage controlled device, where as BJT is a current controlled device.

5. FET'S are much easier to fabricate and are particularly suitable for IC's because they occupy less space than BJT's.

6. FET's are more temperature stable than BJT's.

7. BJT's are cheaper to produce than FET's.

Applications of JFET :-

1. FET is used as a buffer in measuring instruments, receivers since it has high input impedance and low output impedance.

2. FET's are used in RF amplifiers in FM tuners and the communication equipment for the low noise level.

3. Since the input capacitance is low, FET's are used in cascade amplifiers in measuring and test equipments.

4) since the device is Voltage controlled, it is used as a voltage variable resistor in operational amplifiers.

5. FET's are used in mixer circuits in FM and TV receivers

6. FET's are used in oscillator circuits

7. FET's are used in digital circuits in computers, memory circuits because of its small size.

MOSFET (METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR)

METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR is an important semi conductor device and is widely used in many circuit applications.

The input impedance of a MOSFET is much more than that of a JFET because of very small gate leakage current.

Like JFET, MOSFET has Gate, Source and drain. MOSFET is also called IGFET (Insulated gate Field Effect Transistor) because the gate of a MOSFET is insulated from the channel.

MOSFET is clarified in to two types

1. Enhancement type MOSFET
2. Depletion type MOSFET

Principle: By applying a transverse electric field across an insulator, deposited on the semi conducting material

the thickness and hence the resistance of the conducting channel of a semiconducting material can be controlled.

In a depletion MOSFET, the controlling electric field across an insulator, deposited on the semicond-ucting material, the thickness and hence the resistance of a conducting channel reduces the number of majority carriers available for conduction, where as in the enhancement MOSFET, application of MOSFET electric field causes an increase in the number of Majority carriers in the conducting region of a transistor.

<u>Enhancement Type MOSFET</u> :- N channel -

construction and symbol of × Enhancement type MOSFET:

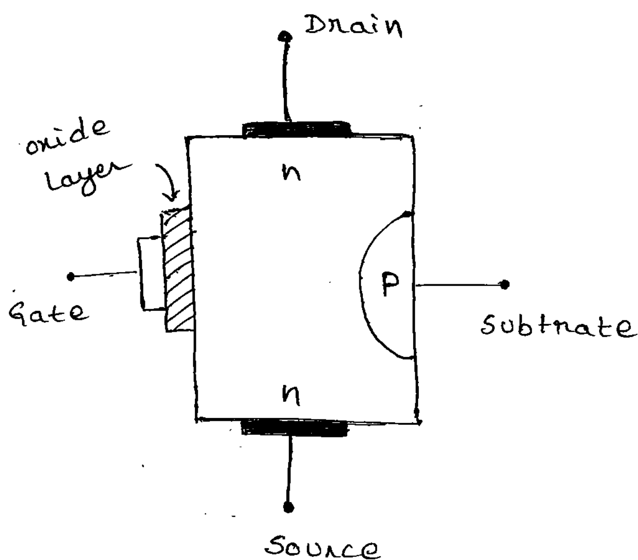
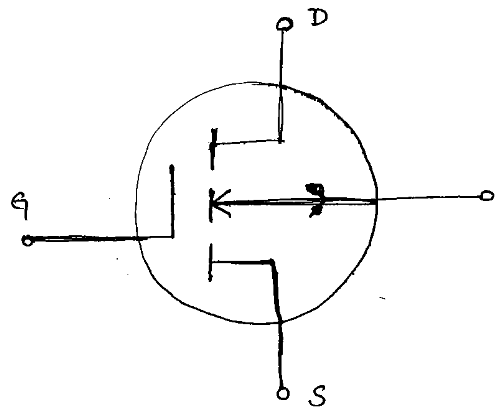


fig (a):

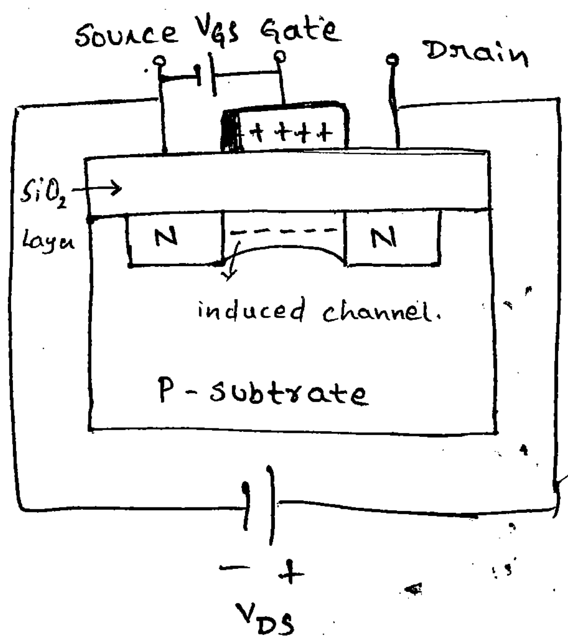


fig(b): Symbol

Fig(a) shows the constructional details of a N-Channel MOSFET. There is only a single P-region. This region is called Subtrate. Two highly doped N-regions are

are diffused in a lightly doped P-type subtrate. one N region is called the source and the other is called drain. A thin insulating layer of SiO_2 is deposited over the surface of the structure and holes are cut into the oxide layer, allowing contact with source and drain. Then a thin layer of Al is formed over the layer of SiO_2. This metal layer covers the entire channel region and it forms the gate G. the metal area of the gate, in conjunction with insulating oxide layer of SiO_2 and the semiconductor channel forms a parallel plate capacitor.

Operation of N-channel Enhancement type MOSFET :



If the subtrate is grounded and a positive voltage is applied at the gate, the positive charge on Gate induces an equal negative charge on

the subtrate side between souce and drain regions.

The negative charge of electrons which are minority carriers in the p-type subtrate forms an inversion layer. As the positive voltage on the gate increases, the induced negative charge in the semi conductor increases. Hence the conductivity increases and current flows from source to drain through the induced channel.

Characteristics of N-channel Enhancement type MOSFET :-

1) Drain characteristics.

The Drain characteristics of N-channel Enhancement type MOSFET is shown in figure below.

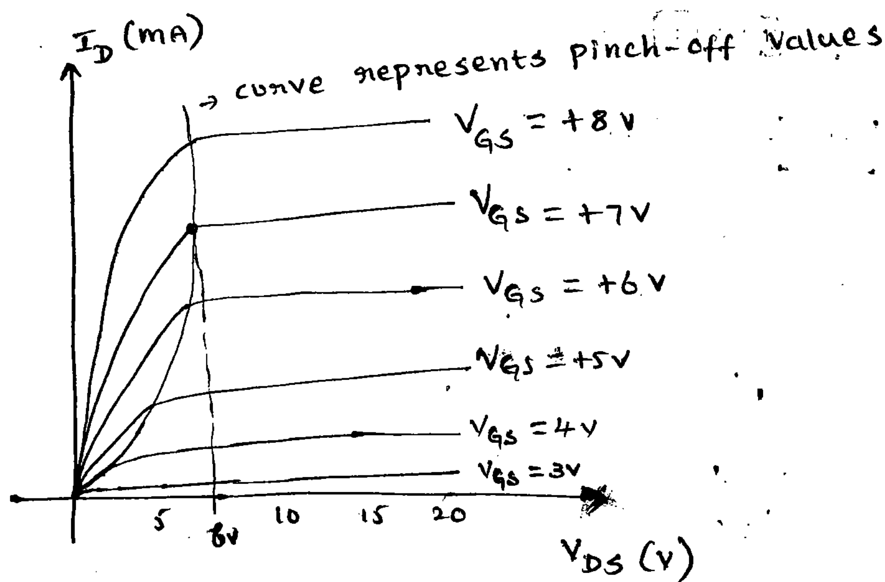


Fig: Drain characteristics

$V_p = 6$ V

$V_{GS} = V_T = 2$ V

2) <u>Transfer characteristics</u> :-

The transfer characteristics of n-channel enhancement type MOSFET is shown in figure below.

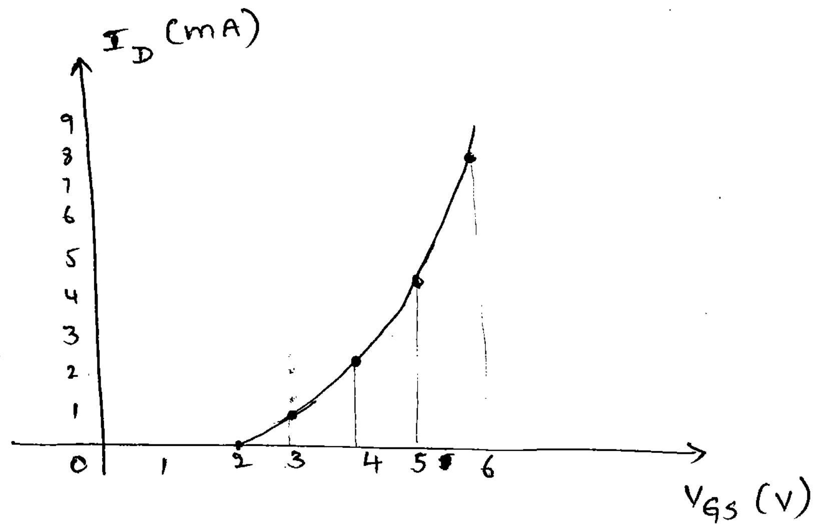


Fig: Transfer characteristics.

2) <u>Depletion type MOSFET</u> :

This is also classified in to two types

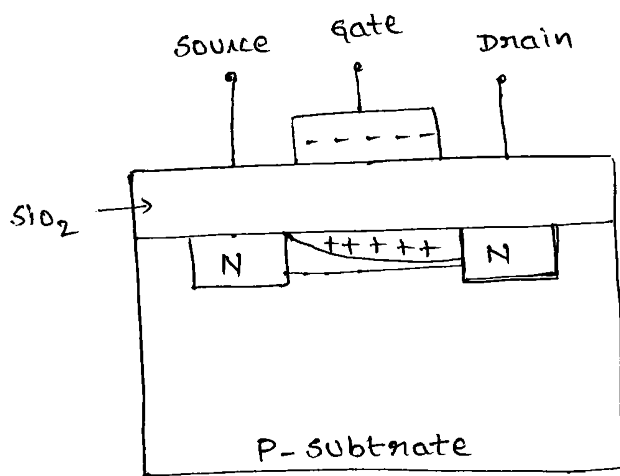
a) N-channel depletion type MOSFET

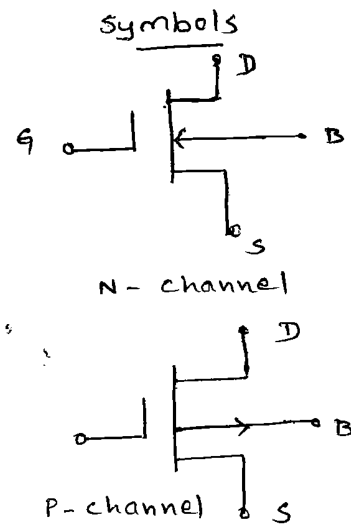
b) P-channel depletion type MOSFET

- <u>N-channel depletion type MOSFET</u> :

<u>Construction</u> :

The construction of an N-channel depletion MOSFET is shown in figure below, where an N-channel is diffused between the source and drain to the basic structure of MOSFET.





when $V_{GS} = 0$ and the drain D at a positive potential with respect to the source, the electrons (majority carriers) flow through the channel from source to drain. therefore, the conventional current I_D flows through the channel from drain to source.

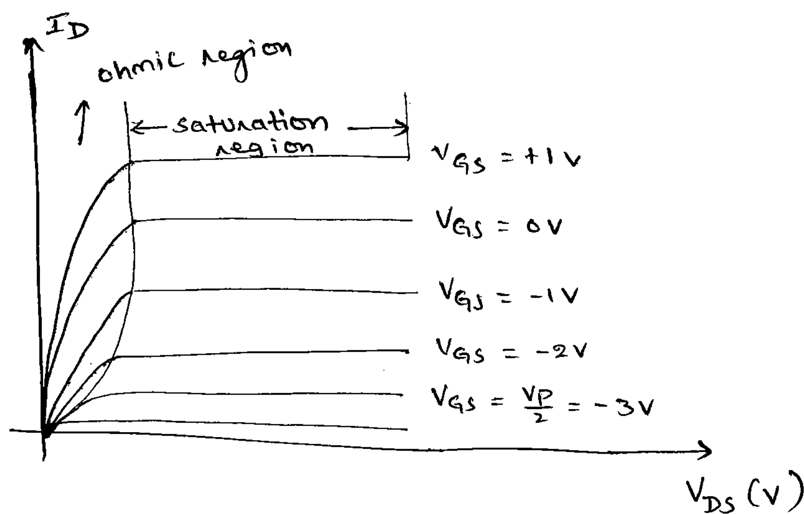
If gate voltage is made negative, positive charge consisting of holes is induced in the channel through SiO_2 of the gate - channel capacitor.

The introduction of the positive charge causes depletion of mobile electrons in the channel. Thus a depletion region is produced in the channel. The shape of the depletion region depends on V_{GS} and V_{DS}. Hence the channel will be wedge shaped as shown in figure.

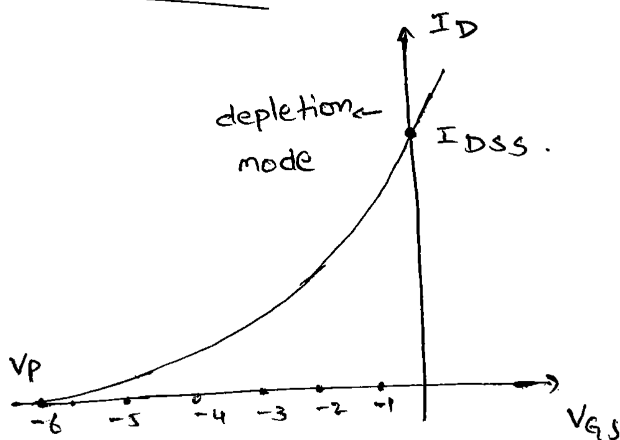
When V_{DS} is increased, I_D increases and it becomes practically constant at a certain value of V_{DS}, called the pinch-off voltage. The drain current I_D almost gets saturated beyond the pinch-off voltage.

The depletion MOSFET can also be operated in an enhancement mode. It is only necessary to apply a positive gate voltage so that negative charges are induced in to the n-type channel. Hence the conductivity of the channel increases and I_D increases.

Drain characteristics of N-channel depletion type MOSFET :



Transfer characteristics :



Comparison of MOSFET with JFET :

1) In enhancement and depletion types of MOSFET, the transverse electric field induced across an insulating layer deposited on the semi conductor material controls the conductivity of the channel. In the JFET the transverse electric field across the reverse biased PN junction controls the conductivity of the channel.

2) The gate leakage current in a MOSFET is of the order of 10^{-12} A. Hence the input resistance of a MOSFET is very high in the order of 10^{10} to 10^{15} Ω. The gate leakage current of a JFET is of the order of 10^{-9} A and its input resistance is of the order of 10^{8} Ω

3) The output characteristics of the JFET are flatter than those of the MOSFET and hence, the drain resistance of a JFET (0.1 to 1MΩ) is much higher than that of a MOSFET (1 to 50KΩ)

4) JFET's are operated only in the depletion mode. The depletion type MOSFET may be operated in both depletion and enhancement mode.

5) Comparing to JFET, MOSFET's are easier to fabricate.

6) MOSFET is very susceptible to overload voltage and

needs special handling during installation. It gets damaged easily if it is not properly handled.

7. MOSFET's are widely used in digital VLSI circuits than JFET's because of their advantages.

Small signal model of JFET :

From the drain and transfer characteristics of the field effect transistor, we can say that, the drain current of an FET is a function of drain to source voltage (V_{DS}) and Gate to Source voltage (V_{GS}). Assuming varying currents and voltages for an FET

$$i_D = f(V_{GS}, V_{DS}) \longrightarrow (1)$$

If both gate and drain voltages are varied, the change in drain current is given approximately by first two terms in the taylor's seris expansion of eq (1)

In small signal notation $\Delta i_D = \left(\frac{\partial i_D}{\partial V_{GS}}\right)_{V_{DS}} \Delta V_{GS} + \left(\frac{\partial i_D}{\partial V_{DS}}\right)_{V_{GS}} \Delta V_{DS}$

$$\Delta i_D = i_d, \quad \Delta V_{GS} = V_{gs} \text{ and } \Delta V_{DS} = V_{ds} \rightarrow (2)$$

So Eq (2) can be written as

$$i_d = g_m V_{gs} + \frac{1}{r_d} V_{ds} \longrightarrow (3)$$

where trans conductance $g_m = \left(\frac{\partial i_D}{\partial V_{GS}}\right)_{V_{DS}} = \left(\frac{\Delta i_D}{\Delta V_{GS}}\right)_{V_{DS}} = \left(\frac{i_d}{V_{gs}}\right)_{V_{DS}} \rightarrow (4)$

and drain resistance $r_d = \left(\frac{\partial V_{DS}}{\partial i_D}\right)_{V_{GS}} \approx \left(\frac{\Delta V_{DS}}{\Delta i_D}\right)_{V_{GS}} = \left(\frac{V_{ds}}{i_d}\right)_{V_{GS}} \rightarrow (5)$

An amplification factor μ for an FET may be defined as

$$\mu = \left(\frac{-\partial V_{DS}}{\partial V_{GS}}\right)_{i_D} = \left(-\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)_{i_D} = \left(\frac{-V_{ds}}{V_{gs}}\right)_{i_d = 0} \rightarrow (6)$$

from Eq (3)
by setting $i_d = 0$, it can be verified that μ, r_d and g_m are related by $\boxed{\mu = r_d\, g_m}$

A small signal model for FET in common source configuration can be drawn satisfying Eq (3) as shown in fig below.

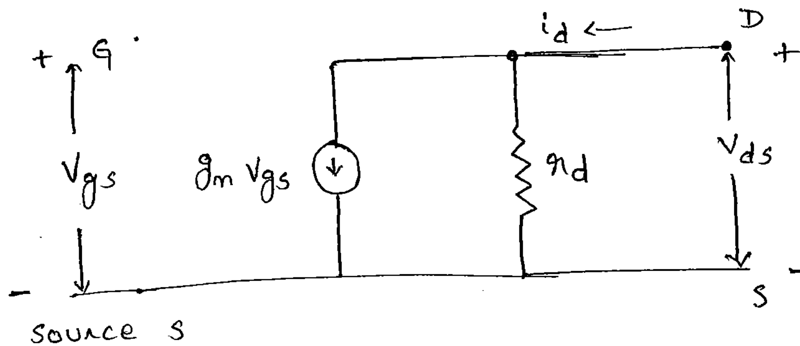


Fig: small signal model for FET in CS configuration

This low frequency model for FET has a Norton's output circuit with a dependent current generator whose magnitude is proportional to the gate to source voltage. The proportionality factor is the transconductance 'g_m'. The output resistance is r_d. The input resistance between the gate and source is infinite, since it is assumed that the reverse biased gate draws no current. For the same reason the resistance between gate and drain is assumed to be infinite.