BIPOLAR JUNCTION TRANSISTOR

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BJT symbol

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Transistor current components

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Input & Output characteristics of a transistor in CE configuration

Input & Output characteristics of a transistor in CC configuration

Comparison of a transistor in CB, CE and CC configurations

BJT specifications

Bipolar junction Transistor (BJT) :-

Introduction :

* A Bipolar junction transistor is a three terminal semi conductor device in which the operation depends on the interaction of majority and minority carriers hence it is named as Bipolar device.

* Transistor means 'Transfer Resistor' ie signals are transfered from low resistance circuit (input) into high resistance (output circuit).

* Basically a third doped element is added to a crystal diode in such a way that two PN junctions are formed. These two junctions give three regions called emitter, base and collector.

* The BJT is analogous to a vaccum triode and is comparatively smaller in size.

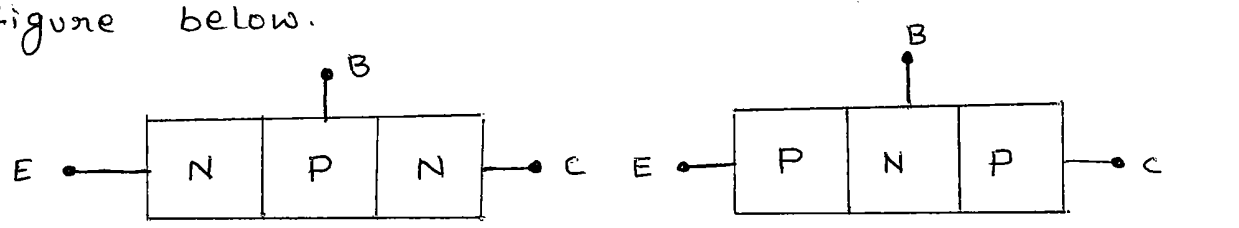
* BJT's are used in amplifier and oscillator circuits and as a switch in digital circuits

BJT construction :-

* The BJT consists of a silicon (Germanium) crystal in which a thin layer of N-type silicon is sandwiched between two layers of P-type silicon. This transistor is referred to as PNP

* similarly, a layer of P-type material is sandwiched between two layers of N-type material this transistor is referred to as NPN.

The two types of BJT are represented in figure below.



(a) NPN Transistor (b) PNP Transistor

* The symbolic representation of the two types of the BJT is shown in figure below.

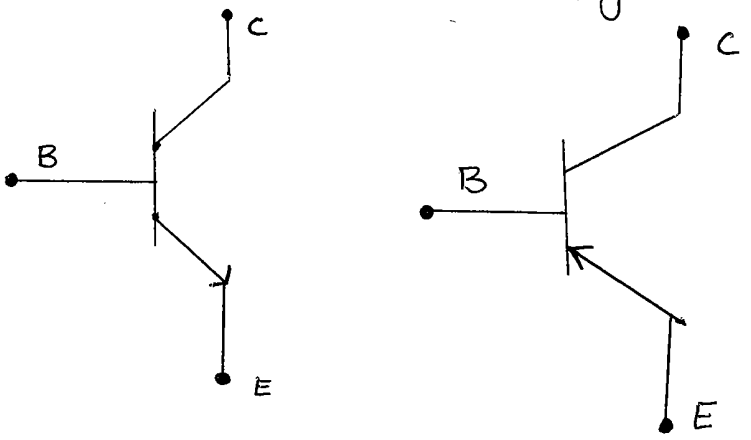


fig (a) Symbol for NPN Transistor

fig(b) Symbol for PNP Transistor.

The three portions of the transistor are Emitter, Base and collector shown as E, B and C respectively. The arrow of the emitter specifies the direction of the current flow when the EB junction is forward biased.

Two junctions are EB → Emitter-base junction
CB → collector-base junction.

Emitter : It is more heavily doped than any of the other region because its main function is to supply majority charge carriers to the base.

Base : Base is lightly doped and very thin. It passes most of the injected charge carriers from the emitter in to the collector.

Collector : collector is moderately doped. Its main function is to collect the majority charge carriers coming from the emitter and passing through the base. In most transistors, collector region is made physically larger than the emitter region because it has to dissipate much greater power.

Transistor Biasing :-

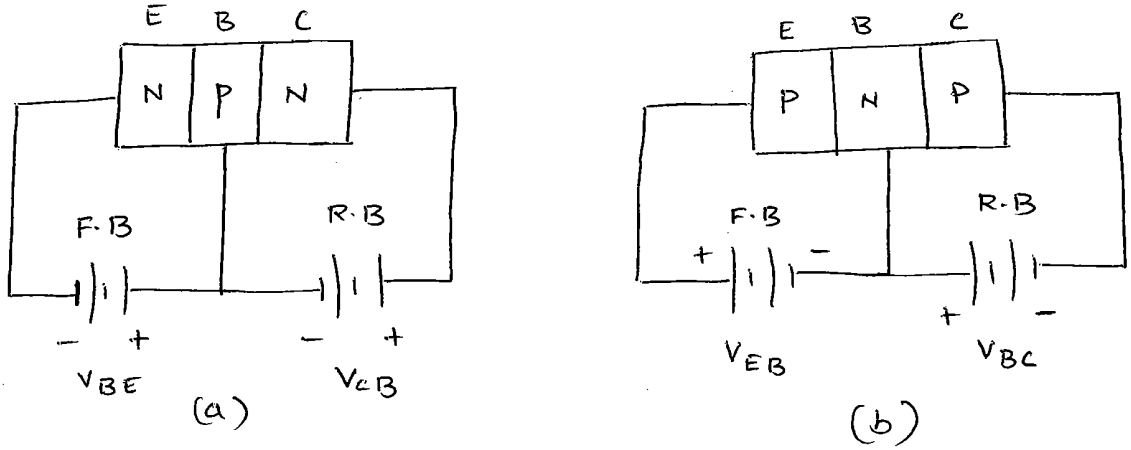
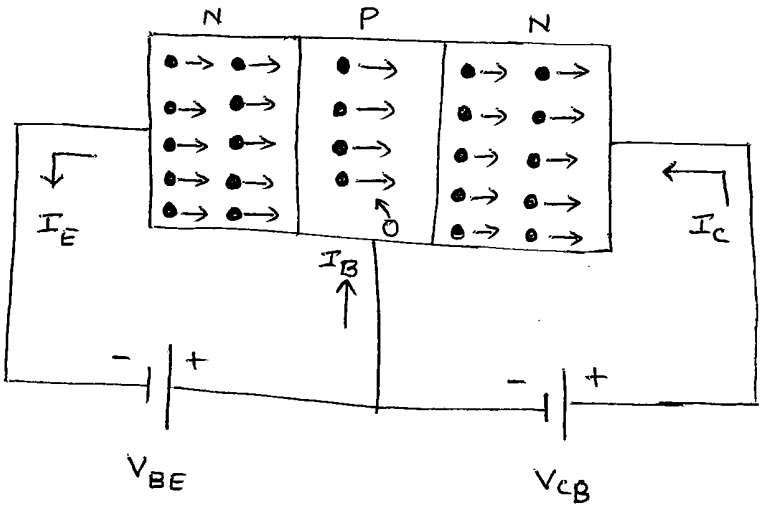


fig: Transistor biasing (a) NPN Transistor and (b) PNP Transistor.

As shown in figure, usually the emitter base junction is forward biased and collector base junction is reverse biased. Due to the forward bias on the emitter base junction, an emitter current flows through the base in to the collector. Though the collector - base junction is reverse biased almost the entire emitter current flows through the collector circuit.

Operation of NPN Transistor :-



As shown in figure, the forward bias is applied to the emitter base junction of an NPN transistor causes a lot of electrons from the emitter region to cross over to the base region.

As the base is lightly doped with P-type impurity, the number of holes in the base region is very small and hence the number of electrons that combine with holes in the P-type base region is also very small. Hence a few electrons combine

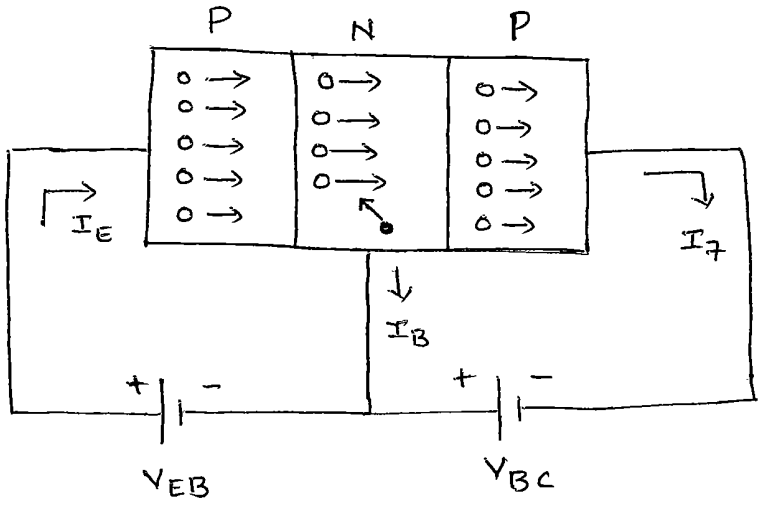
with holes to constitute a base current I_B. The remaining electrons (more than 95%) crossover into the collector region to constitute a collector current (I_C). Thus the base and collector current summed up gives the emitter current. ie

$$I_E = -(I_C + I_B) \quad \left[\because \text{As per KCL } I_C + I_B + I_E = 0 \right]$$

In the external circuit of the NPN bipolar junction transistor, the magnitudes of emitter current I_E, the base current I_B and the collector current I_C are related by

$$\boxed{I_E = I_C + I_B}$$

Operation of PNP Transistor :-



As shown in figure above, the forward bias applied to the emitter base junction of a PNP transistor causes a lot of holes from the emitter region to crossover to the base region.

As the base is lightly doped with N-type impurity, the number of electrons in the base region are very small and hence the number of holes combined with electrons in the N-type region is also very small. Hence a few holes combined with electrons to constitute a base current I_B. The remaining holes (more than 95 %) cross over in to the collector region to constitute a collector current I_C. Thus the collector and base current when summed up gives the emitter current

$$\text{ie } I_E = -(I_C + I_B)$$

In the external circuit of the PNP bipolar junction transistor, the magnitudes of the emitter current I_E, the base current I_B and the collector current I_C are related by

$$\boxed{I_E = I_C + I_B}$$

Current components in a transistor:

The figure below shows the various current components which flow across the forward biased emitter junction and reverse biased collector junction in P.N.P Transistor.

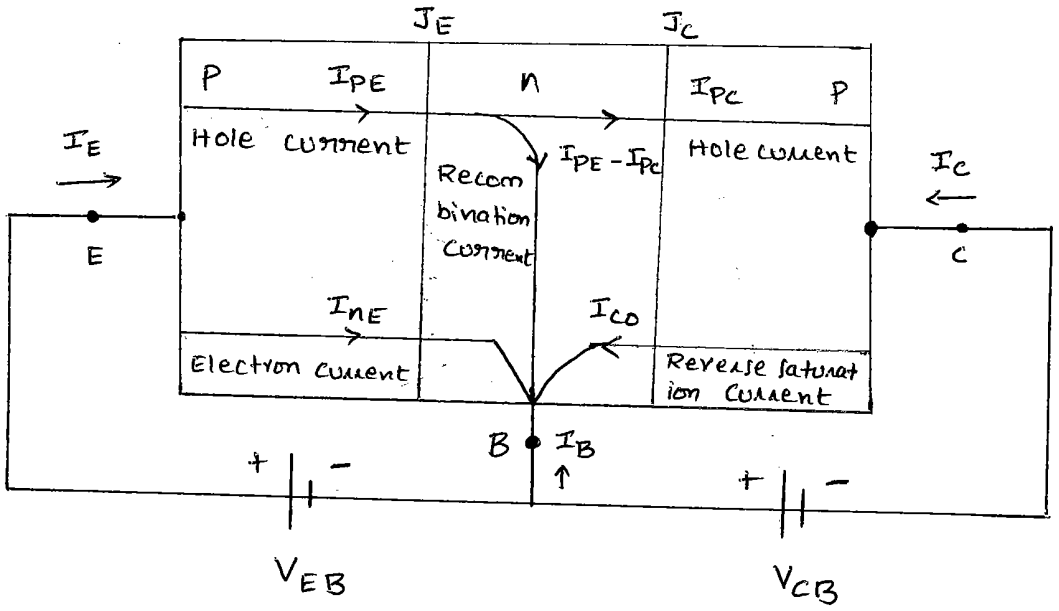


Figure: current components in a transistor with forward biased emitter and reverse biased collector junctions.

The emitter current consists of the following two parts.

1) Hole current I_{PE} constituted by holes (holes crossing from emitter into base

2) Electron current I_{nE} constituted by electrons (electrons crossing from base in to the emitter)

Therefore total emitter current

$$I_E = I_{PE}\ (\text{majority}) + I_{nE}\ (\text{minority})$$

The holes crossing the emitter base junction J_E reaching the collector base junction J_C constitutes collector current I_{PC}.

Not all the holes crossing the emitter base junction reach collector base junction J_C

because some of them combine with the electrons in the n-type base

Since base width is very small, most of the holes cross the collector base junction J_c and very few recombine, constituting the base current ($I_{pE} - I_{pc}$)

When the emitter is open circuited, $I_E = 0$ and hence $I_{pc} = 0$. Under this condition, the base and collector together current I_c equals the reverse saturation current I_{co}, which consists of the following two parts.

1) I_{pco} caused by the holes moving across I_c from N region to P region

2) I_{nco} caused by electrons moving across I_c from P-region to N-region.

$$\therefore I_{co} = I_{nco} + I_{pco}$$

In general $I_C = I_{nc} + I_{pc}$

Thus for a PNP Transistor

$$\boxed{I_E = I_B + I_C}$$

Transistor circuit configurations :

Basically there are three types of circuit connections for operating a transistor.

① common base configuration (CB)

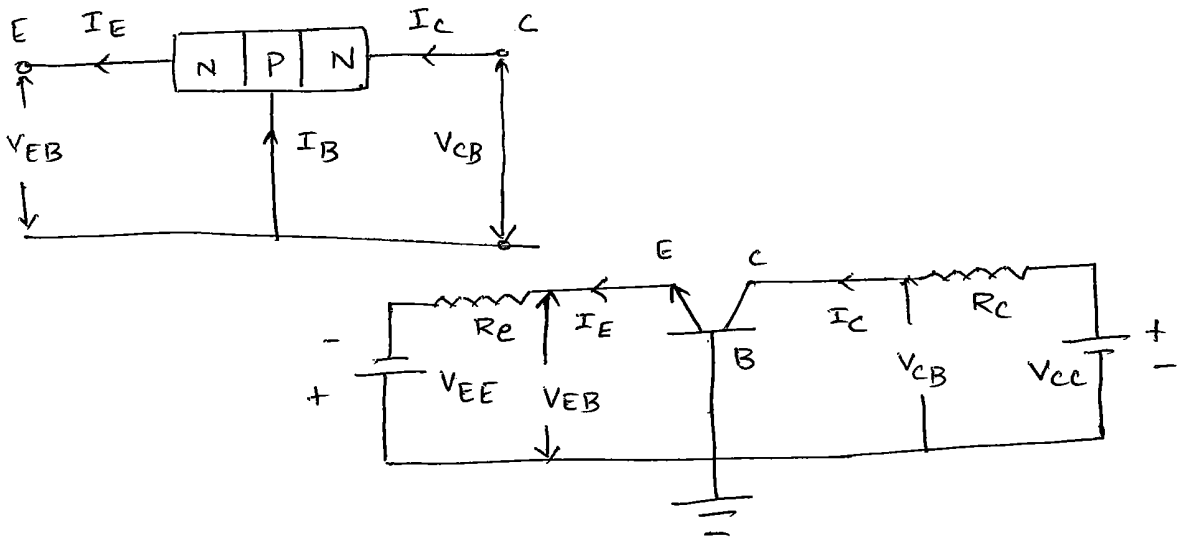
② common emitter configuration (CE)

③ common collector configuration (cc)

① CB configuration :

This is also called grounded base configuration. In this configuration, emitter is the input terminal, collector is the output terminal and base is the common terminal.

The input signal is applied between the emitter and base where as output is taken out from the collector and base, thus emitter current is the input current and collector current is the output current.



The ratio of collector current to emitter current is called <u>dc current gain</u> (α_{dc} or α) of a transistor

$$\alpha = -\frac{I_C}{I_E} \Rightarrow \boxed{I_C = -\alpha I_E}$$

The negative sign indicates that emitter and collector currents flow in opposite direction (ie. the conventional emitter current flows out and collector current enters in to the transistor)

Thus α of a transistor is a measure of the quality of a transistor, higher the value of α, better the transistor in the sense that the collector current more closely equal to the emitter current. Its value ranges from 0.98 to 0.985.

For simplicity $I_C = \alpha I_E$

we know that $I_E = I_C + I_B$

$$I_B = I_E - \alpha I_E$$

$$\boxed{I_B = (1-\alpha) I_E}$$

Ac current gain $\alpha_{ac} = \frac{-\Delta I_C}{\Delta I_E}$

(It refers to the change in collector current to change in emitter current)

<u>Total collector current</u> :-

The whole emitter current does not reach the collector because a small percentage of electron hole combination occuring in the base area

it gives rise to base current. Due to reverse biasing of collector base junction wide depletion region is formed across it, this depletion region helps the minority carriers of base (electrons) to cross the collector base junction. thus more collector current flows in addition to this leakage current (I_{CBO}) Therefore total collector current is given by

$$I_C = \alpha I_E + I_{CBO}$$

where I_{CBO} = leakage current. Hence it is very small hence it is neglected in circuit calculation.

Characteristics of CB Configuration :-

The circuit diagram for determining the static characteristics of an NPN Transistor in the common base configuration is shown in figure below.

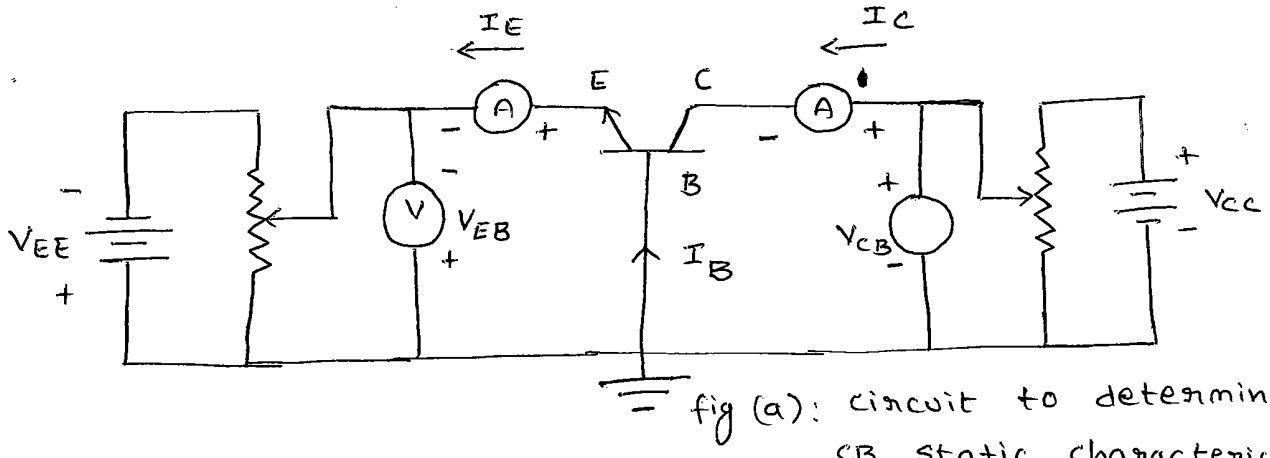
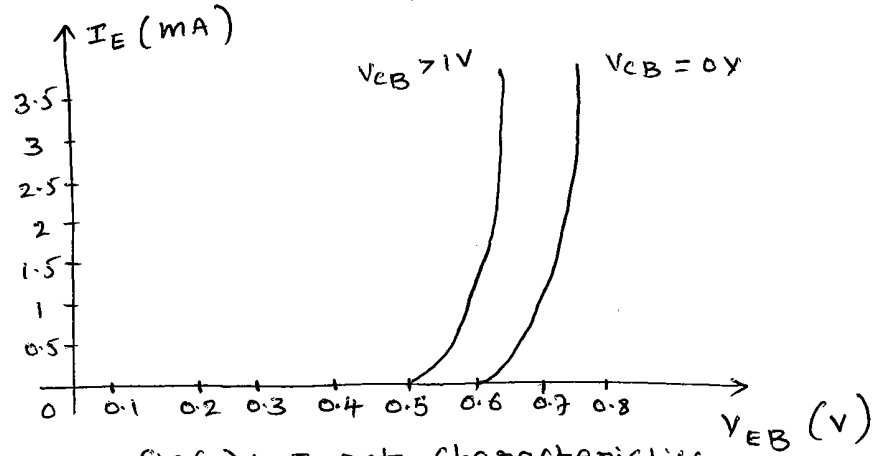


fig (a): circuit to determine CB static characteristics

Input characteristics :-

To determine the input characteristics the collector base voltage V_{CB} is kept constant at zero volt and the emitter current I_E is increased from zero in suitable equal steps by increasing V_{EB}

this is repeated for higher fixed values of V_{CB}. A curve is drawn between emitter current (I_E) and emitter base voltage (V_{EB}) at constant collector base voltage (V_{CB}). The input characteristics thus obtained are shown in figure below.



fig(b): Input Characteristics

when V_{CB} is equal to zero and the emitter base junction is forward biased as shown in the characteristics, the junction behaves as a forward biased diode so that emitter current (I_E) increases rapidly with small increase in emitter base voltage (V_{EB})

when V_{CB} is increased keeping V_{EB} constant, the width of the base region will decrease. This effect results in an increase of I_E. Therefore the curve shift ~~two~~ towards the left as V_{CB} is increased.

<u>output Characteristics</u> :- To determine the output characteristics, the emitter current I_E is kept constant at a suitable value by adjusting the

the emitter - base voltage (V_{EB}). Then V_{CB} is increased in suitable equal steps and the collector current I_C is noted for each value of I_E. This is repeated for different fixed values of I_E. Now the curves of I_C versus V_{CB} are plotted for constant values of I_E and the output characteristics thus obtained is shown in figure below.

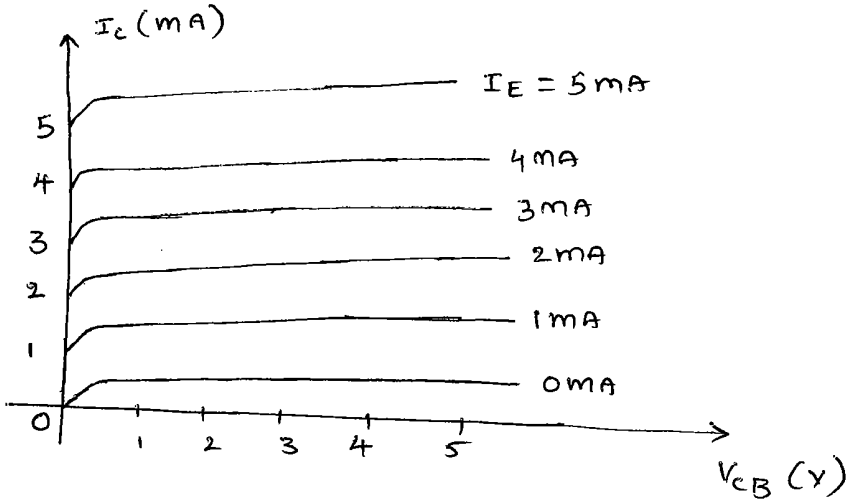


fig C:- CB output characteristics

From the characteristics, it is seen that for a constant value of I_E, I_C is independent of V_{CB} and the curves are parallel to the axis of V_{CB}.

I_C flows even when V_{CB} is equal to zero. As the emitter base junction is forward biased, the majority carriers ie electrons, from the emitter are injected in to the base region. Due to the action of the internal potential barrior at the reverse biased collector base junction, they flow to the collector region and gives rise to I_C even when V_{CB} is equal to zero.

Early effect or base-width modulation :-

As the collector voltage V_{cc} is made to increase the reverse bias, the depletion region width between collector and base tends to increase, with the result that the effective width of the base decreases. This dependency of base width on collector to emitter voltage is known as the 'Early Effect'. This decrease in effective base-width has three consequences.

(1) There is a less chance for recombination within the base region. Hence α increases with increasing $|V_{CB}|$

(2) The charge gradient is increased within the base, and consequently, the current of minority carriers injected across the emitter junction increases.

(3) For extremely large voltages, the effective base width may be reduced to zero, causing voltage break down in the transistor. This phenomenon is called the "punch through."

For higher values of V_{CB}, due to Early effect, the value of α increases. for example α changes from 0.98 to 0.985. Hence there is a very small positive slope in the CB output characteristics and hence the output resistance is not zero.

Transitor parameters :-

The slope of the CB characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common base hybrid parameters or h-parameters.

(i) Input impedance (h_{ib}) : It is defined as the ratio of the change in (input) emitter voltage to change in (input) emitter current with the (output) collector voltage V_{CB} kept constant. Therefore

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}, \quad V_{CB} \text{ constant.}$$

It is the slope of CB input characteristics I_E versus V_{EB} as shown in fig(b). The typical value of h_{ib} ranges from 20Ω to 50Ω.

(ii) output admittance (h_{ob}) : It is defined as the ratio of change in the (output) collector current to the corresponding change in collector voltage with the emitter current I_E (input) kept constant.

$$\therefore \quad hob = \frac{\Delta I_C}{\Delta V_{CB}}, \quad I_E \text{ constant.}$$

It is the slope of CB output characteristics I_C versus V_{CB} as shown in fig(c). The typical value of this parameter is of the order 0.1 to 10 μ mhos.

3) Forward current gain (h_{fb}) :

It is defined as a ratio of the change in the collector current (output) to the corresponding change in emitter current (input) keeping the collector voltage (output) V_{CB} constant Hence

$$h_{fb} = \frac{\Delta I_C}{\Delta I_E}, \quad V_{CB} \text{ constant.}$$

It is the slope of I_C versus I_E curve. Its typical value varies from 0.9 to 1.

(iv) Reverse voltage gain (h_{rb}) : It is defined as the ratio of the change in the emitter voltage (input) and the corresponding change in collector voltage (output) with constant emitter current (I_E). Hence

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}, \quad I_E \text{ constant.}$$

It is the slope of V_{EB} versus V_{CB} curve. Its typical value is of the order of 10^{-5} to 10^{-4}.

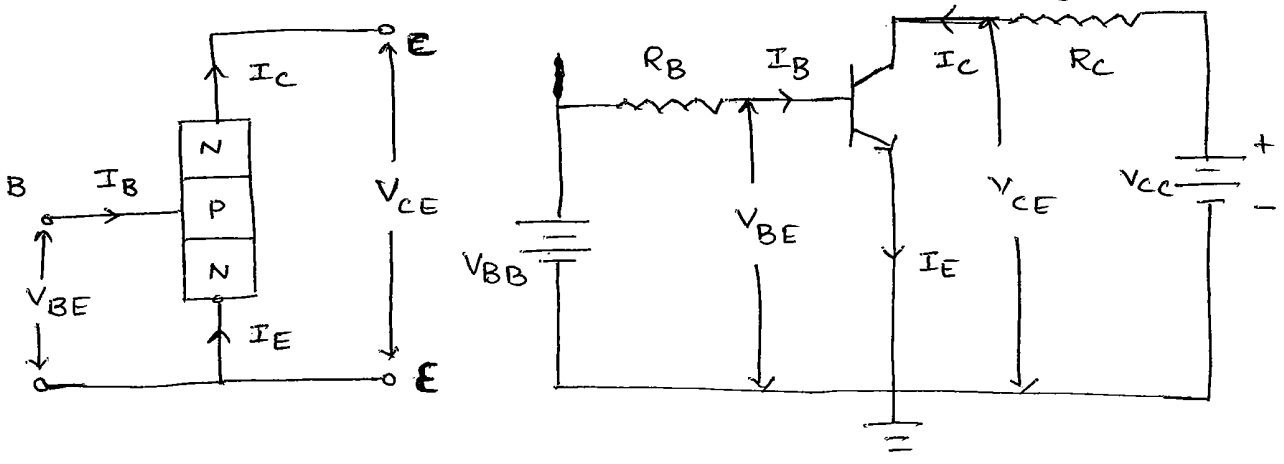
2) Common emitter configuration (CE) :

CE configuration means the emitter terminal is common to the input and output. In this case input signal is applied between the base and emitter and output signal is taken out from the collector and emitter terminals.

The ratio of dc collector current (output) to the dc base current (input) is called the dc current gain (β_{dc} or β).

$$\beta = \frac{I_C}{I_B}$$

The collector current of a transistor is much larger than the base current. Therefore the value of β is much greater than unity.



Relation between α and β :-

$$\beta = \frac{I_C}{I_B} \quad \text{and} \quad \alpha = \frac{I_C}{I_E} \Rightarrow \frac{\beta}{\alpha} = \frac{I_E}{I_B}$$

we know that $I_B = I_E - I_C$

$$\therefore \beta = \frac{I_C}{I_E - I_C} = \frac{\frac{I_C}{I_E}}{1 - \frac{I_C}{I_E}} = \frac{\alpha}{1-\alpha}$$

So $\boxed{\beta = \frac{\alpha}{1-\alpha}}$ from this we can calculate for α

$$\therefore \boxed{\alpha = \frac{\beta}{1+\beta}}$$

Total collector current :-

In CE configuration I_B is the input current and I_C is the output current.

we know that $I_E = I_C + I_B$

but $I_C = \alpha I_E + I_{CBO}$

$$I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$I_C (1-\alpha) = \alpha I_B + I_{CBO}$$

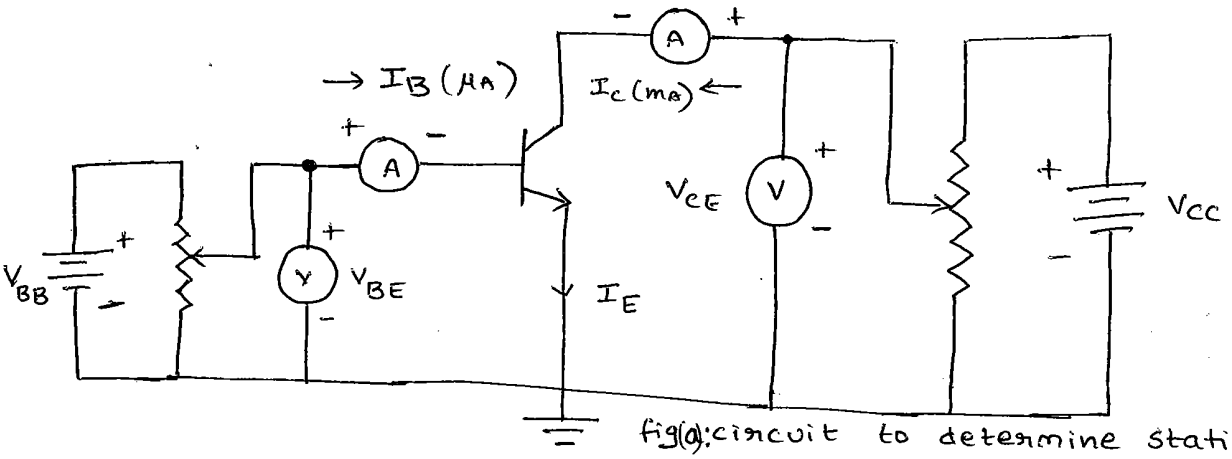
$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

$$I_C = \beta I_B + I_{CEO}$$

where $\beta = \frac{\alpha}{1-\alpha}$, I_{CEO} = Leakage current in CE configuration

$$\therefore \boxed{I_C = \beta I_B + I_{CEO}}$$

Common Emitter Configuration (CE) Characteristics :-

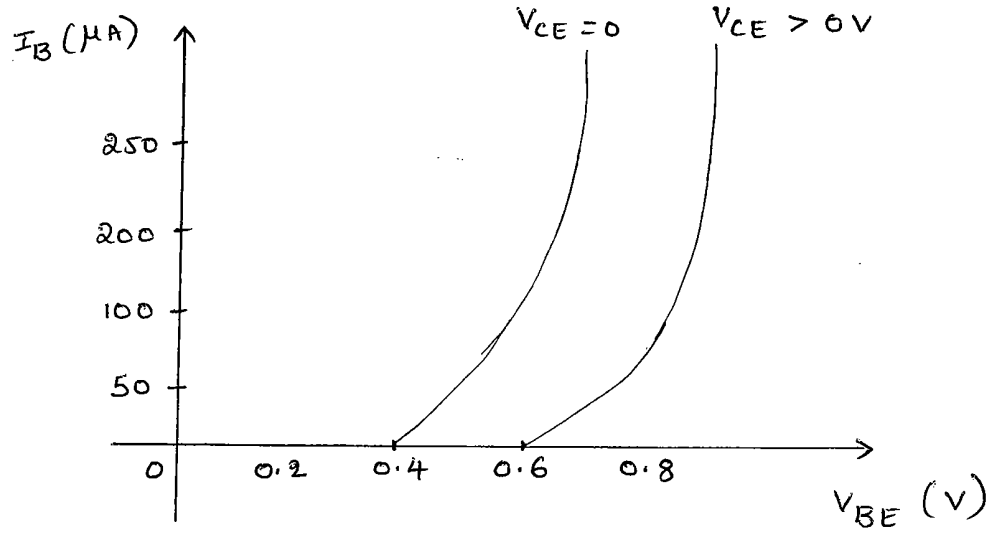


fig(a): circuit to determine static chars in CE configuration

The circuit diagram for determining the static characteristics curves of an NPN transistor in the common Emitter configuration is shown in figure above.

Input characteristics :-

To determine the input characteristics, the collector to emitter voltage is kept constant at zero volt and base current is increased from zero in equal steps by increasing V_{BE} in the circuit shown in fig(a).



fig(b): CE input characteristics.

The value of V_{BE} is noted for each setting of I_B. This procedure is repeated for higher fixed values of V_{CE}, and the curves of I_B Vs V_{BE} are drawn. The input characteristics thus obtained are shown in ~~above~~ fig (b).

When $V_{CE} = 0$, the emitter - base junction is forward biased and the junction behaves as a forward biased diode. Hence the input characteristic for $V_{CE} = 0$ is similar to that of a forward - biased diode.

When V_{CE} is increased, the width of the depletion region at the reverse biased collector - base junction will increase. Hence the effective width of the base will decrease. This effect causes a decrease in the base current (I_B). Hence to get the same value of I_B as that for $V_{CE} = 0$, V_{BE} should be increased. Therefore the curve shifts to the right as V_{CE} increases.

Output Characteristics :-

To determine the output characteristics, the base current I_B is kept constant at a suitable value by adjusting base - emitter voltage V_{BE}.

The magnitude of collector - emitter voltage (V_{CE}) is increased in suitable equal steps from zero

and the collector current I_C is noted for each setting of V_{CE}. Now the curves of I_C versus V_{CE} are plotted for different constant values of I_B. The output characteristics thus obtained are shown in fig (c) below

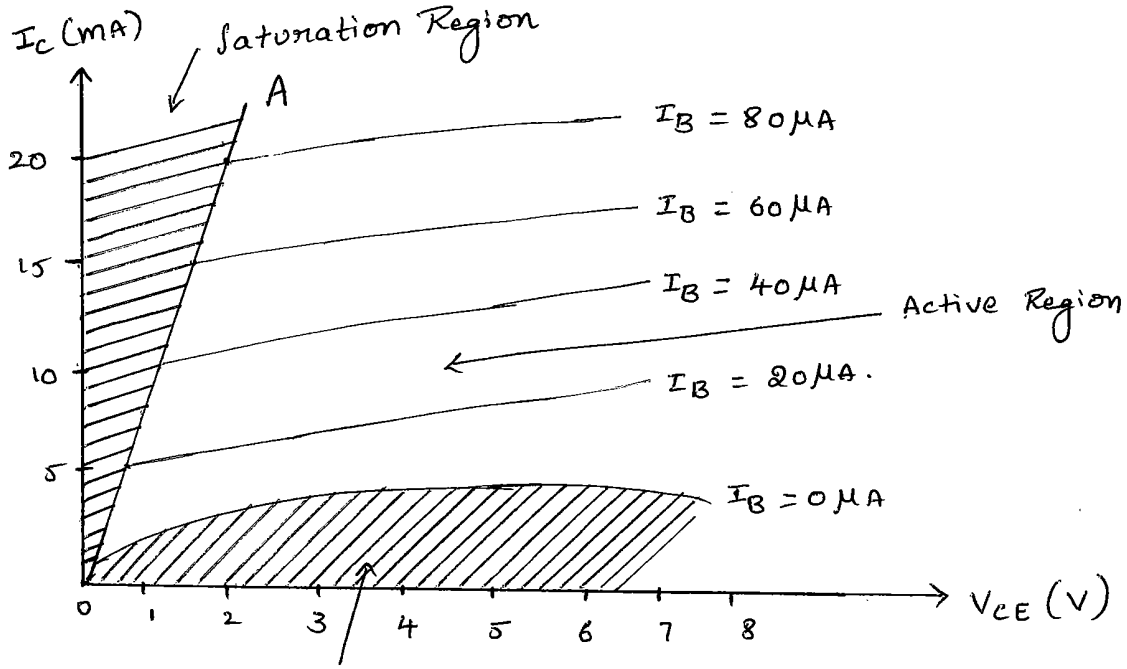


fig c : output characteristics.

we know that $\beta = \frac{\alpha}{1-\alpha}$

For larger values of V_{CE}, due to early effect, a very small change in α is reflected in a very large change in β.

For example $\alpha = 0.98$ then $\beta = \frac{0.98}{1-0.98} = 49$

If α increases to 0.985, then $\beta = \frac{0.985}{1-0.985} = 66$.

Here a slight increase in α by about 0.5% results in an increase in β by about 34%.

Hence the output characteristics of CE configuration show a larger slope when compared with CB configu-ration.

The output characteristics have three regions

① Saturation region

② cut off region

③ Active region.

① Saturation Region :-

The region of curves to the left of the line OA is called the saturation region (hatched) and the line OA is called the saturation line. In this region both junctions are forward biased and an increase in base current doesn't cause a corresponding large change in I_C. The ratio of $V_{CE(sat)}$ to I_C in this region is called saturation resistance.

② cut-off region :-

The region below the curve for $I_B = 0$ is called the cut-off region (hatched) In this region both junctions are reverse biased. When the operating point for the transistors enter the cut-off region, the transistor is off. Hence the collector current becomes almost zero and the collector voltage almost equals V_{cc}. The transistor is virtually an open circuit between collector and emitter.

3) Active Region:-

The central region where the curves are uniform in spacing and slope is called the 'active region (unhatched). In this region emitter base junction is forward biased and the collector base junction is reverse biased. If the transistor is to be used as a linear amplifier, it should be operated in the active region.

→ If the base current is subsequently driven large and positive, the transistor switches in to the saturation region via the active region.

→ In this ON condition large collector current flows and collector voltage falls to a very low value called $V_{CE\,sat}$, typically around 0.2 V for a Si transistor. The transistor is virtually a short circuit in this state.

Transistor parameters:-

The slope of the CE characteristics will give the following four transistor parameters. Since these parameters have different dimensions they are commonly known as common emitter hybrid parameters or h parameters.

(i) Input impedance (hie) :-

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}, \quad V_{CE} \text{ constant.}$$

It is the slope of CE input characteristics I_B Versus V_{BE} as shown in fig(b). The typical value of h_{ie} ranges from 500 to 2000 Ω.

(ii) Output admittance (h_{oe}) :-

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}, \quad I_B \text{ constant.}$$

It is the slope of of CE output characteristics I_C versus V_{CE} as shown in fig(c). the typical value of this parameter is of the order of 0.1 to 10 μmhos.

(iii) Forward current gain (h_{fe}) :-

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}, \quad V_{CE} \text{ constant.}$$

It is the slope of I_C versus I_B curve. Its typical value varies from 20 to 200.

(iv) Reverse voltage gain (h_{re}) :-

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}, \quad I_B \text{ constant.}$$

It is the slope of V_{BE} versus V_{CE} curve. Its typical value is of the order of 10^{-5} to 10^{-4}.

3) Common collector configuration (CC) :-

CC configuration means the collector terminal is common to the input and output. In this case input signal is applied between the base and collector and output signal is taken out from the emitter and collector terminals.

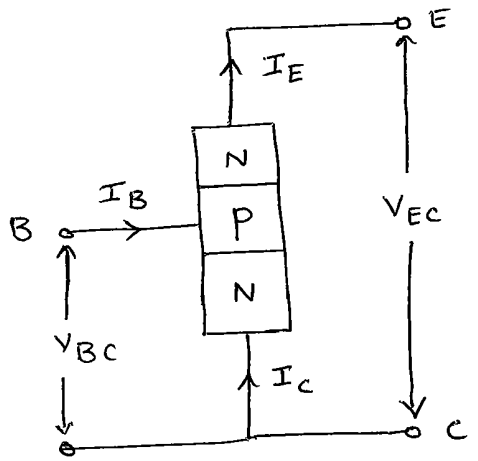
The ratio of emitter current ($\frac{\text{output}}{\text{input}}$) to the base current ($\frac{\text{in}}{\text{put}}$) is called the dc current gain (γ_{dc} or γ).

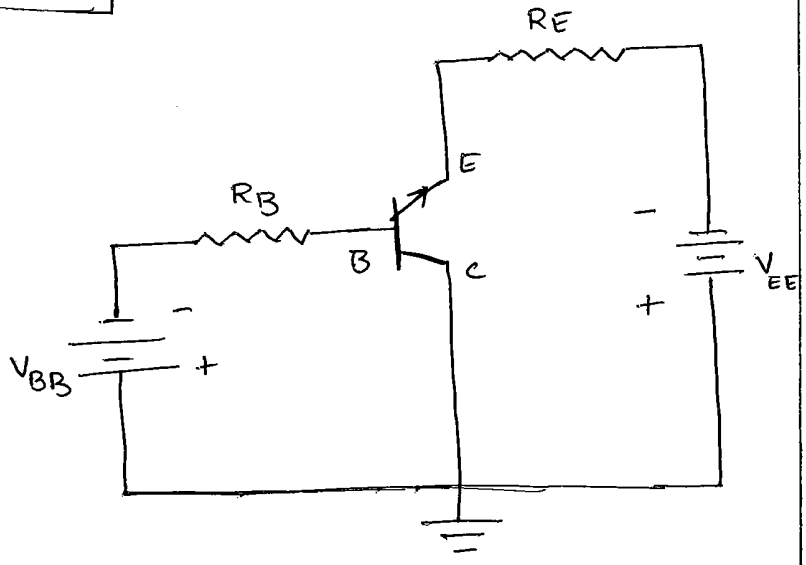
$$\therefore \quad \gamma = \frac{I_E}{I_B}$$

$$\gamma = \frac{I_E}{I_B} = \frac{I_E}{I_C}\,\frac{I_C}{I_B} = \frac{1}{\alpha} \cdot \beta = \frac{\beta}{\alpha}$$

$$\gamma = \frac{\beta}{\alpha} = \frac{\beta}{\beta/1+\beta} = 1+\beta$$

$$\therefore \quad \boxed{\gamma = \frac{1}{1-\alpha} = 1+\beta}$$





Total Emitter current :

We know that $I_C = \alpha I_E + I_{CBO}$

and $I_E = I_C + I_B$

$$I_E = I_B + \alpha I_E + I_{CBO}$$

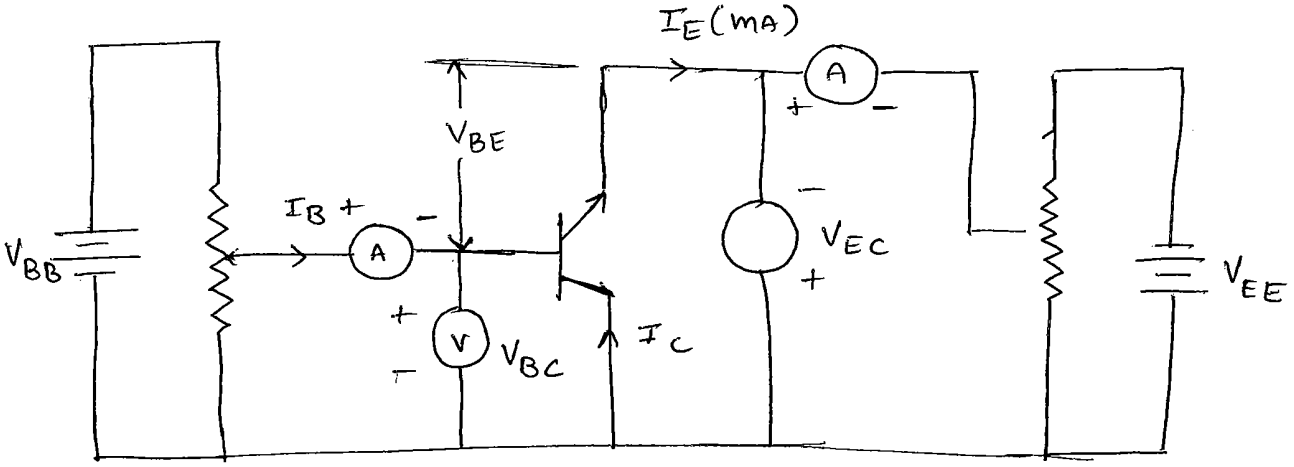
$$I_E(1-\alpha) = I_B + I_{CBO}$$

$$I_E = \frac{1}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

$$I_E = (\beta+1) I_B + (\beta+1) I_{CBO}$$

Characteristics of CC configuration :-

The circuit diagram for determining the static characteristics of an NPN transistor in the common collector configuration. is shown in figure below.

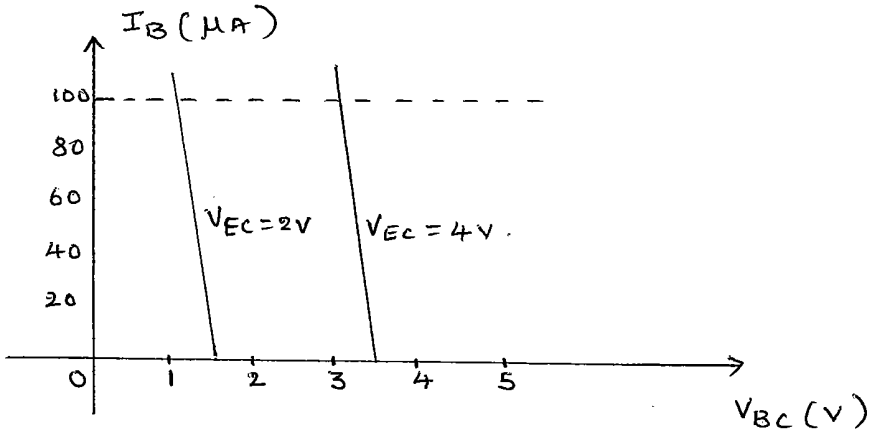


fig(a) circuit to determine cc static char's

Input characteristics :-

To determine the input characteristics V_{EC} is kept at a suitable fixed value.

Then V_{BC} is increased in equal steps and the corresponding increase in I_B is noted. This is repeated for different fixed values of V_{EC}. The input characteristics are plotted below.



fig(b) : CC input characteristics

The common collector input characteristics are different from CB and CE configurations. The difference is due to the fact that V_{BC} is determined by V_{EC}. This is because when the transistor is biased on, V_{BE} remains around 0.7 V, (for Si) and 0.3 for Ge and V_{EC} may be much larger than 0.7 V

from fig(a) $V_{EC} = V_{BC} + V_{BE}$

$$V_{BE} = V_{EC} - V_{BC}$$

If $V_{EC} = 2V$ at $I_B = 100\mu A$ then

$$V_{BC} = V_{EC} - V_{BE} = 2 - 0.7 = 1.3\,V.$$

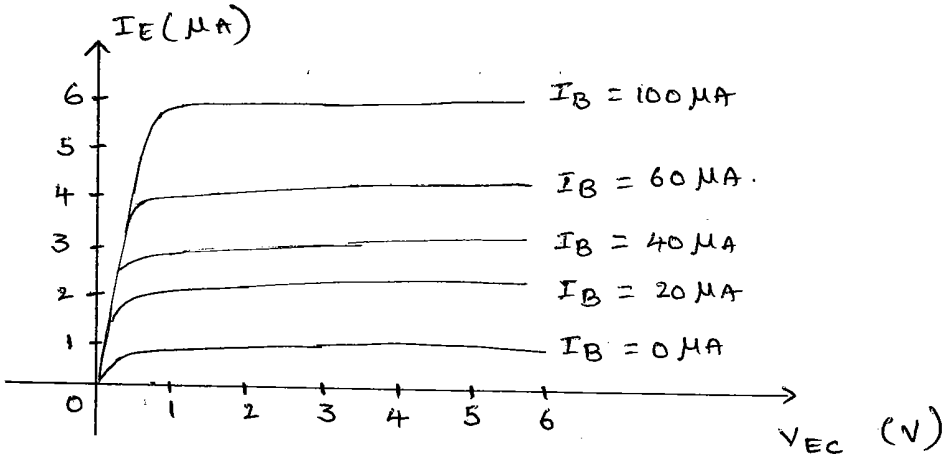
Suppose V_{EC} is maintained constant at 2V, while the input voltage V_{BC} is increased to 1.5 V then V_{BE} is reduced to 0.5 V. Because of V_{BE} is reduced,

I_B is reduced from 100μA to zero.

Output characteristics :

The cc output characteristics are plotted, I_E versus V_{EC} for several fixed values of I_B.

We know that the CE output characteristics are plotted b/n I_C and V_{CE}. since I_C is approximately equal to I_E thus cc o/p characteristics is identical to CE output characteristics.



fig(c) : cc output characteristics.

Current Amplification factor :-

In a transistor amplifier with a.c input signal, the ratio of change in output current to the change in input current is known as the current amplification factor.

In the CB configuration the current amplification factor $\alpha = \frac{\Delta I_C}{\Delta I_E}$ ⟶ (1)

In the CE configuration the current amplification factor $\beta = \frac{\Delta I_C}{\Delta I_B}$ ⟶ (2)

In the CC configuration the current amplification factor $\gamma = \frac{\Delta I_E}{\Delta I_B}$ ⟶ (3)

Relationship between α and β

we know that $\Delta I_E = \Delta I_C + \Delta I_B$ ⟶ (4)

By definition $\Delta I_C = \alpha \Delta I_E$ (from Eq (1))

ie $\Delta I_E = \alpha \Delta I_E + \Delta I_B$

$\Delta I_B = \Delta I_E (1-\alpha)$ ⟶ (5)

Dividing both sides by ΔI_C, we get

$$\frac{\Delta I_B}{\Delta I_C} = \frac{\Delta I_E}{\Delta I_C}(1-\alpha)$$

$$\Rightarrow \frac{1}{\beta} = \frac{1}{\alpha}(1-\alpha) \quad \Rightarrow \beta = \frac{\alpha}{1-\alpha}$$

Re arranging we also get $\alpha = \frac{\beta}{1+\beta}$ (or) $\frac{1}{\alpha} - \frac{1}{\beta} = 1$

From this relationship, it is clear that as α approaches unity, β approaches infinity. The CE configuration is used for almost all transistor applications because of its high current gain β.

Relation among α, β and γ :

In the CC transistor amplifier circuit, I_B is the input current and I_E is the output current.

from Eq (3) $\gamma = \frac{\Delta I_E}{\Delta I_B}$

Substituting $\Delta I_B = \Delta I_E - \Delta I_C$, we get

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C} \longrightarrow (6)$$

~~Diving~~ Dividing the numerator and denominator of eq (6) by ΔI_E, we get

$$\gamma = \frac{\frac{\Delta I_E}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha}$$

$$\therefore \quad \gamma = \frac{1}{1-\alpha} \longrightarrow (7)$$

$$\gamma = \frac{1}{1-\alpha} = \frac{1}{1 - \frac{\beta}{1+\beta}} = \frac{1+\beta}{1+\beta-\beta} = 1+\beta$$

$$\therefore \boxed{\gamma = \frac{1}{1-\alpha} = 1+\beta}$$

Comparison of CB, CE and CC configurations

Property	CB	CE	CC
Input resistance	Low (about 100 Ω)	Moderate (about 750 Ω)	High (750)
output resistance	High (450 KΩ)	Moderate (45 KΩ)	low (25 Ω)
Current gain	1	High	High
voltage gain	About 150	About 500.	Less than 1
phase shift b/n i/p and o/p voltages	0 (or) 360°	180°	0 (or) 360°
Applications	For high frequency circuits	for audio frequency ckts	For impedance matching

BJT specifications :-

In different conditions such as active, saturation and cut-off there are different junction voltages. The junction voltages for a typical npn transistor at 25°C are given in the table below.

Type	$V_{CE\,sat}$	$V_{BE\,sat}$	$V_{BE\,active}$	$V_{BE\,cut\,in}$	$V_{BE\,cutoff}$
Si	0.3	0.7	0.7	0.5	0.0
Ge	0.1	0.3	0.3	0.1	-0.1

The junction voltages in the above table are appropriate for an npn transistor. For Pnp transistor the signs of all entries should be reversed.

TRANSISTOR BIASING AND STABILIZATION

Need for biasing

Operating point

DC and AC load lines

Bias stabilization

Fixed bias

Collector to base bias

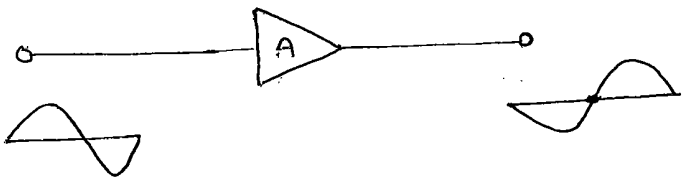
Voltage divider bias

Bias compensation

Introduction :

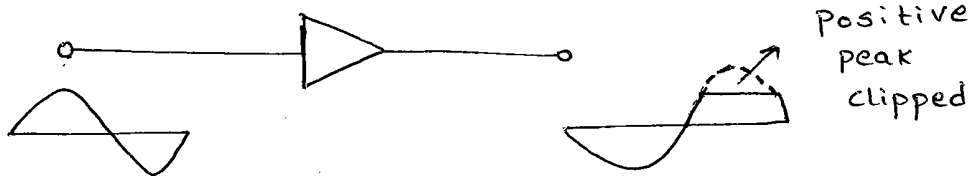
The transistors are used in a large variety of applications and in many ways. To use a transistor in any application, it is necessary to provide the sufficient voltage and current to switch ON and to operate in active region (Linear) of its transfer characteristics. This process is known as "Biasing".

(i)



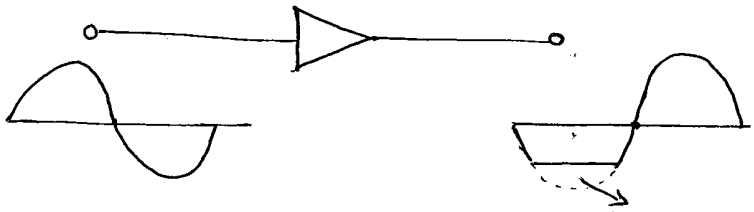
fig(a): Amplifier biased at active region.
(faithful amplification)

(ii)



fig(b): Amplifier biased at cut-off region.
(unfaithful ~~faithful~~ amplification)

(iii)



fig(c): Amplifier biased at Saturation region
(unfaithful amplification)

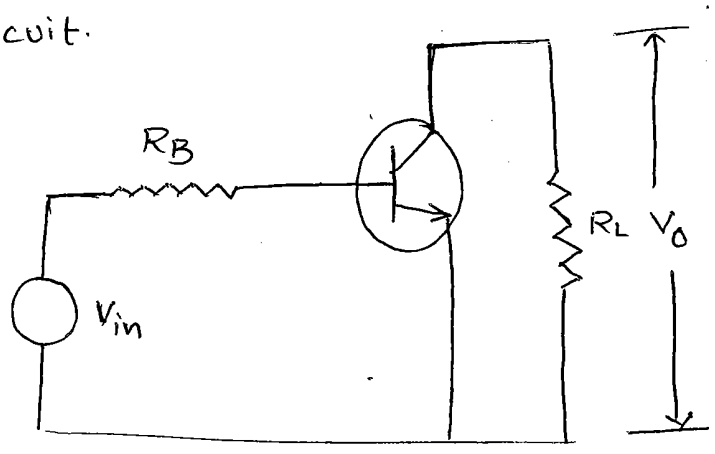
Fig: Different levels of biasing.

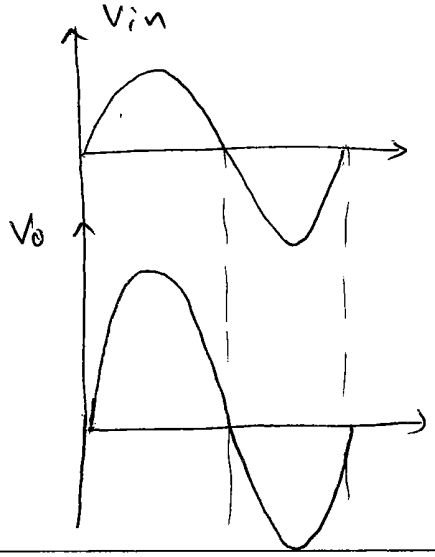
In other words biasing means providing a fixed or minimum amount of the current which would flow through the transistor with the desired fixed voltage across the transistor junctions. The proper values of these currents and voltages allow a transistor to work in the Linear region and it amplify the weak signal faithfully.

The faithful amplification means, the transistor must increase the magnitude of the signal without changing its shape. (shown in fig (a)).

Need for Biasing :-

when an a.c input signal is applied to the circuit shown in figure below, during positive half cycle of input, the emitter base junction becomes forward biased results in current flows from emitter to base then base to collector circuit.





During the negative half cycle of input, the junction becomes reverse biased, so no current flows in the circuit, results in negative half cycle is not amplified The resultant output is unfaithful or distorted.

Thus to obtain faithful amplification, the following three conditions must be satisfied.

1) The emitter base junction should be properly forward biased
2) the collector base junction should be reverse biased.
3) There should be proper zero signal collector current.

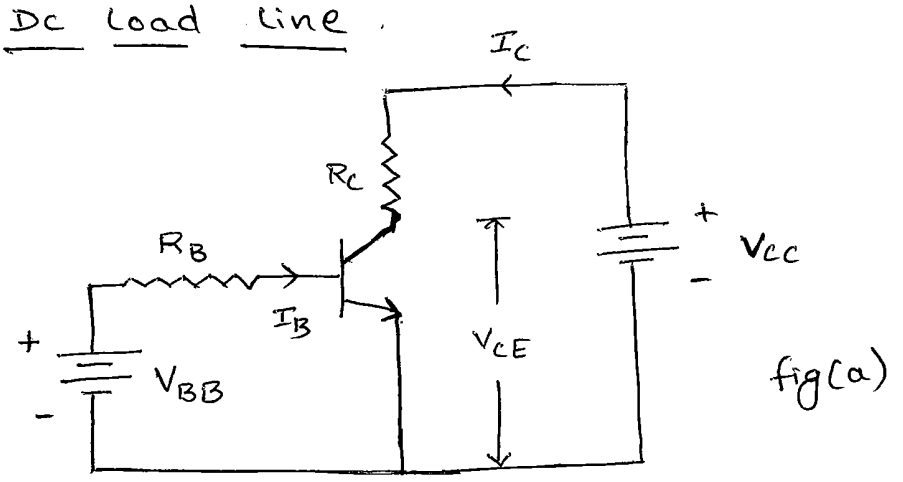
The proper flow of zero signal dc collector current and the maintenance of proper collector - emitter voltage during the passage of signal is known as 'transistor biasing'.

Operating point :-

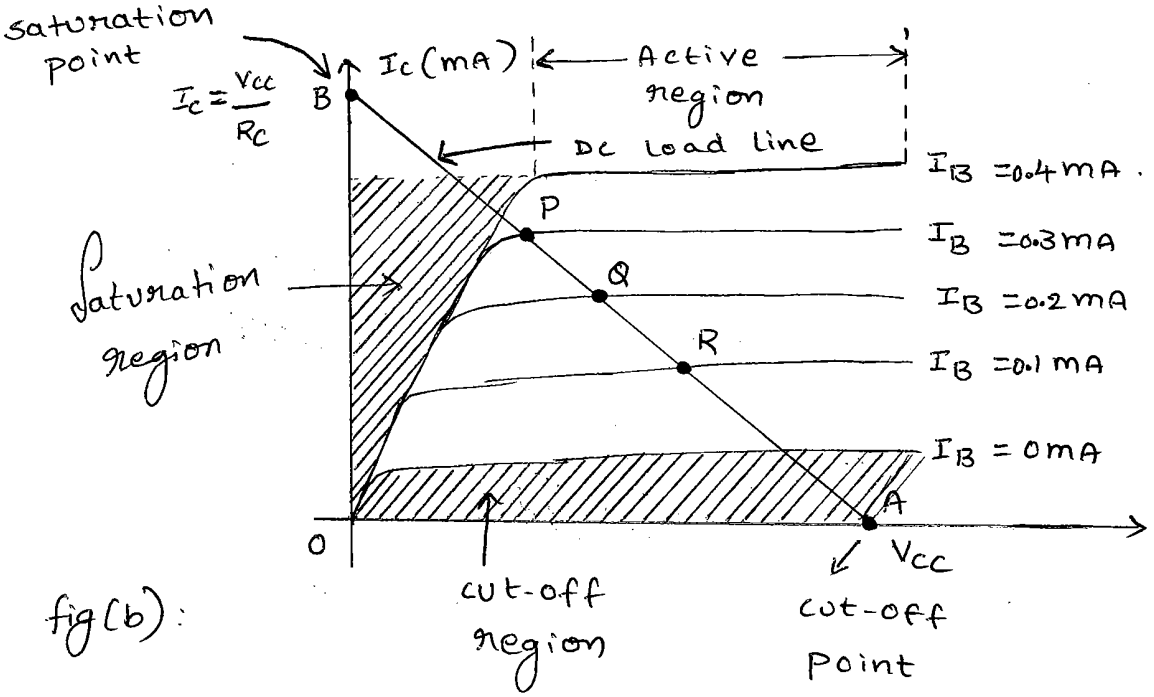
In order to produce distortion - free output in amplifier circuits, the supply voltages and resistances in the circuit must be suitably choosen. These voltages and resistances establish a set of d.c voltage V_{CEQ} and current I_{CQ} to

operate the transistor in the active region. These voltages and currents ~~are called~~ define ~~quiescent values~~ the point at which the transistor operates. This point is called ~~the~~ as operating point or Q point or Quiescent point.

Dc load line.



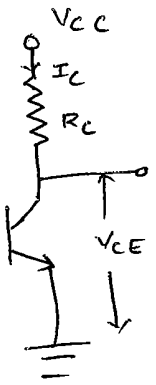
fig(a)



fig(b):

consider common emitter configuration circuit shown in fig(a).

In transistor circuit analysis generally it is required to determine the value of I_C for the desired value of V_{CE}. From the load line method we can determine the value of I_C for any of ~~the~~ desired value of V_{CE}. The output characteristics of CE configuration is shown in fig(b).



Apply KVL to the output circuit

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C .$$

→ If the bias voltage V_{BB} is such that the transistor is not conducting then $I_C = 0$ and $V_{CE} = V_{CC}$. Therefore when $I_C = 0$, $V_{CE} = V_{CC}$ this point is plotted on the output characteristics as point A.

→ If $V_{CE} = 0$ then $I_C = \frac{V_{CC}}{R_C}$.

Therefore, $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C}$. this point is plotted on the output characteristics as point B the line draw through these points is straight line called '<u>d.c load line</u>'

The d.c load line is plot of I_C versus V_{CE} for a given value of V_{CC}. Hence from the load line we can determine the I_C for any desired value of V_{CE}.

Ex: If $I_B = 0.2\ mA$ Assume $\beta = 100$

We know $\beta = \frac{I_C}{I_B} \Rightarrow I_C = \beta I_B$

$I_C = 100 \times 0.2\ mA$

$I_C = 20\ mA$.

$V_{CC} = I_C R_C + V_{CE}$ [Assume $V_{CC} = 10\ V$, $R_C = 200\Omega$]

$V_{CE} = V_{CC} - I_C R_C$

$V_{CE} = 10 - \left[(20 \times 10^{-3}) \times 200 \right] = 10 - 4 = 6\ V$

$\therefore V_{CE} = 6\ V$

These values of I_C and V_{CE} defines Q. point, marked as Q on the output characteristics.

Operating Point (or) Quiescent point :

In designing a circuit, a point on the Load line is selected as the dc bias point (or) Quiescent point. The Q. point specifies the collector current I_C and collector to emitter voltage V_{CE} that exists when no input signal is applied.

The dc bias point (or) Quiescent point is the point on the load line which represents the current in a transistor and the voltage across it when no ~~signal~~ input signal is applied.

The dc bias point (or) quiescent point is the point on the load line which represents the current in a transistor and the voltage across it when no signal is applied. The zero signal values of I_C and V_{CE} are known as the operating point.

Biasing: The process of giving proper supply voltages and resistances for obtaining the desired Q-point is called biasing.

→ How to choose the operating point on DC load line:-

The transistor acts as an amplifier when it is operated in active region. After the d.c conditions are established in the circuit, when an a.c signal is applied to the input, the base current varies according to the amplitude of the signal and causes I_C to vary consequently producing an output voltage variation.

Consider point 'P' which is very near to the saturation point, even though the base current is varying sinusoidally the output current and output voltage is seen to be clipped at the positive peaks. This results in distortion of the signal.

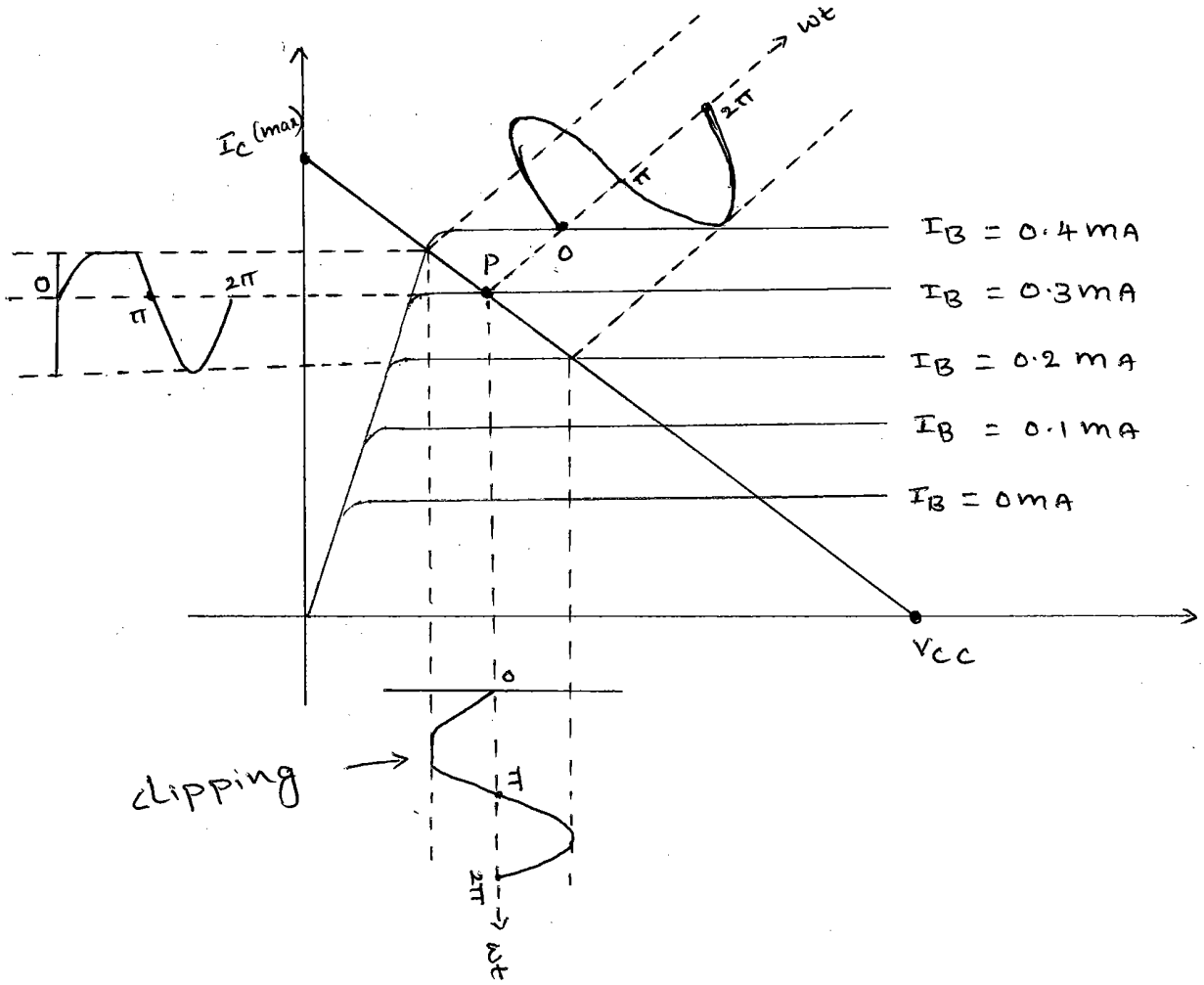


Fig: operating point near saturation region gives clipping at the positive peak.

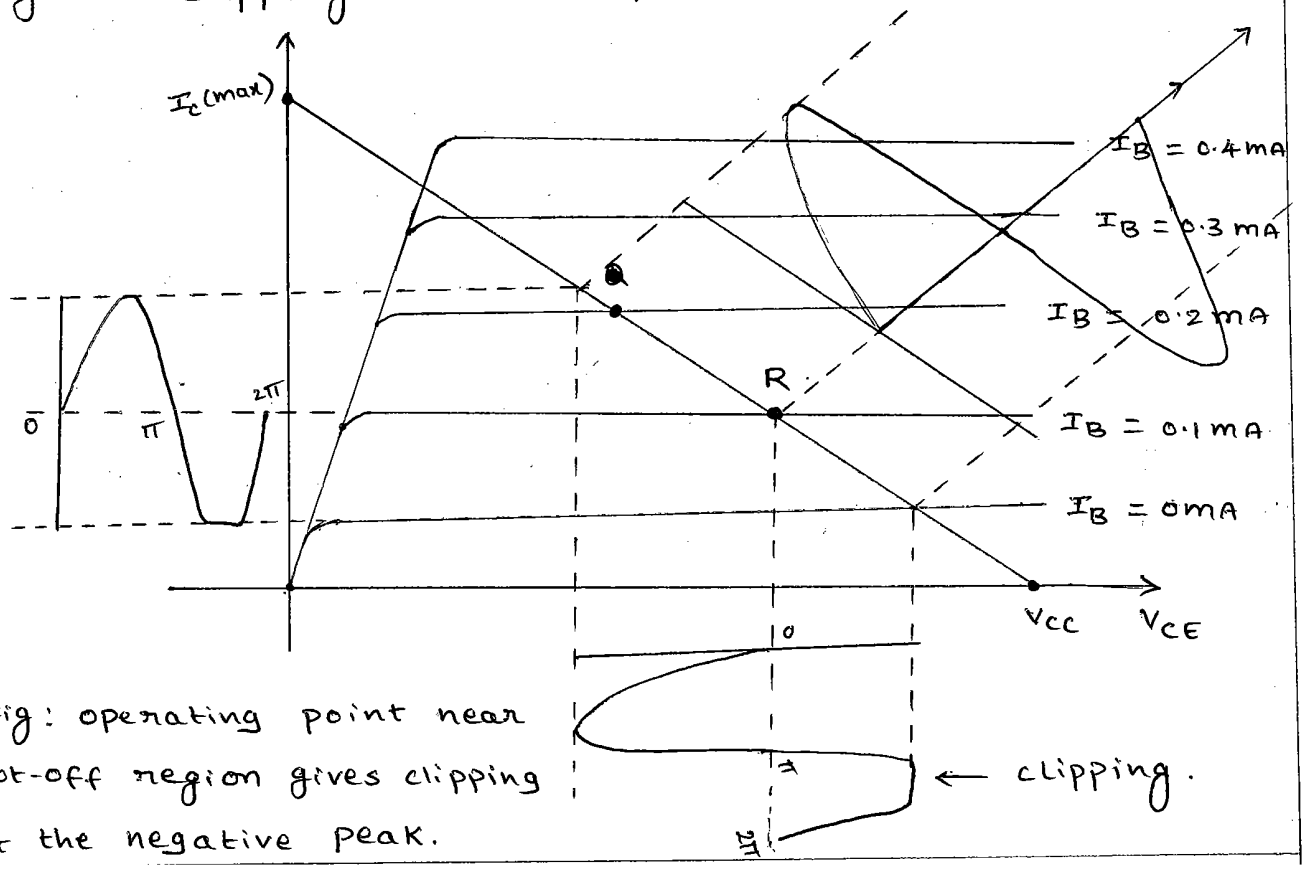


Fig: operating point near cut-off region gives clipping at the negative peak.

consider point R which is very near to the cut-off region. The output signal is now clipped at the negative peak. Hence this is also not a suitable operating point.

consider point Q which is the mid point of the DC load line then the output signal will not be distorted.

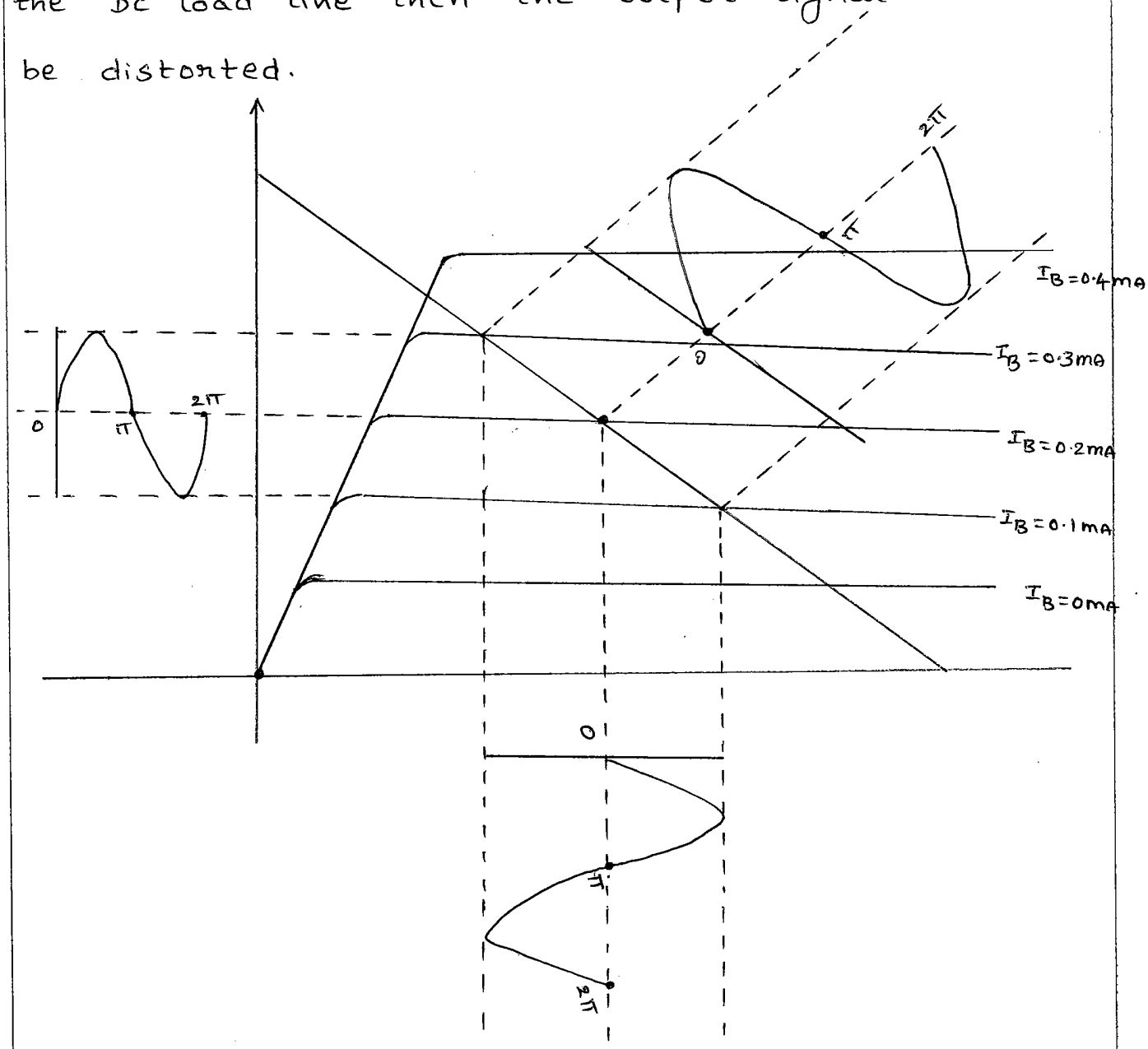


fig: operating point at the center of active region is most suitable.

A good amplifier amplifies signals without introducing distortion. Thus always the operating point is chosen as the mid point of the DC load line.

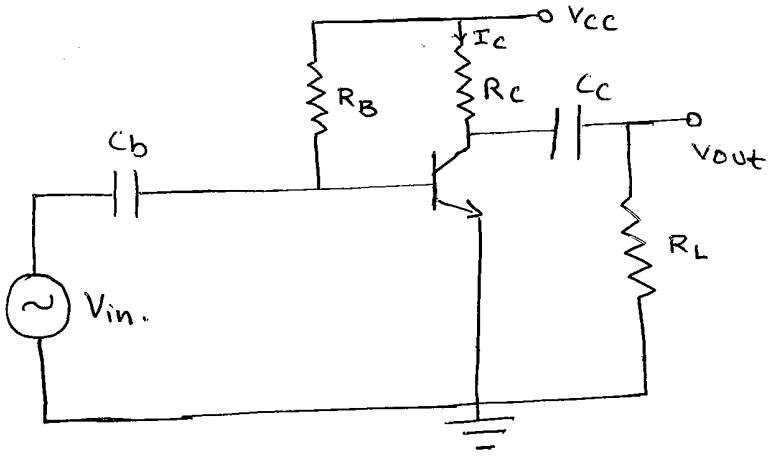
Ac Load Line :-

→ The dc load line is drawn when no input ac signal is applied to the circuit.

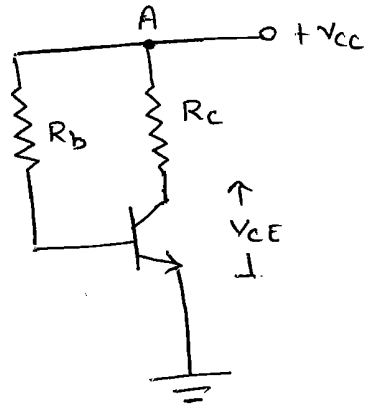
→ If an ac signal is applied to the circuit then the collector current and collector emitter voltage is changed, hence we obtain a load line called "ac load line".

→ The a.c load line can be defined as line on the output characteristics which gives the values of I_C and V_{CE} when a.c input signal is applied.

→ The practical biasing circuit in CE Configuration is shown in figure below.



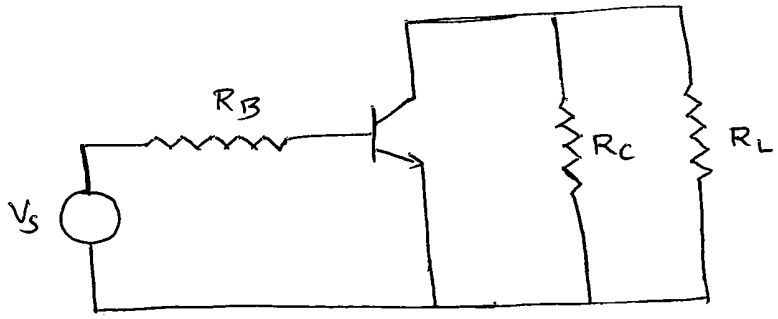
fig(a) : Practical CE Amplifier



fig(b): DC equivalent circuit.

To obtain dc equivalent circuit assume all the capacitors act as open circuited and thus a.c source resistance and load resistance R_L is not included in the circuit. thus the resultant Equivalent dc circuit is shown ~~below~~. in fig(b) above

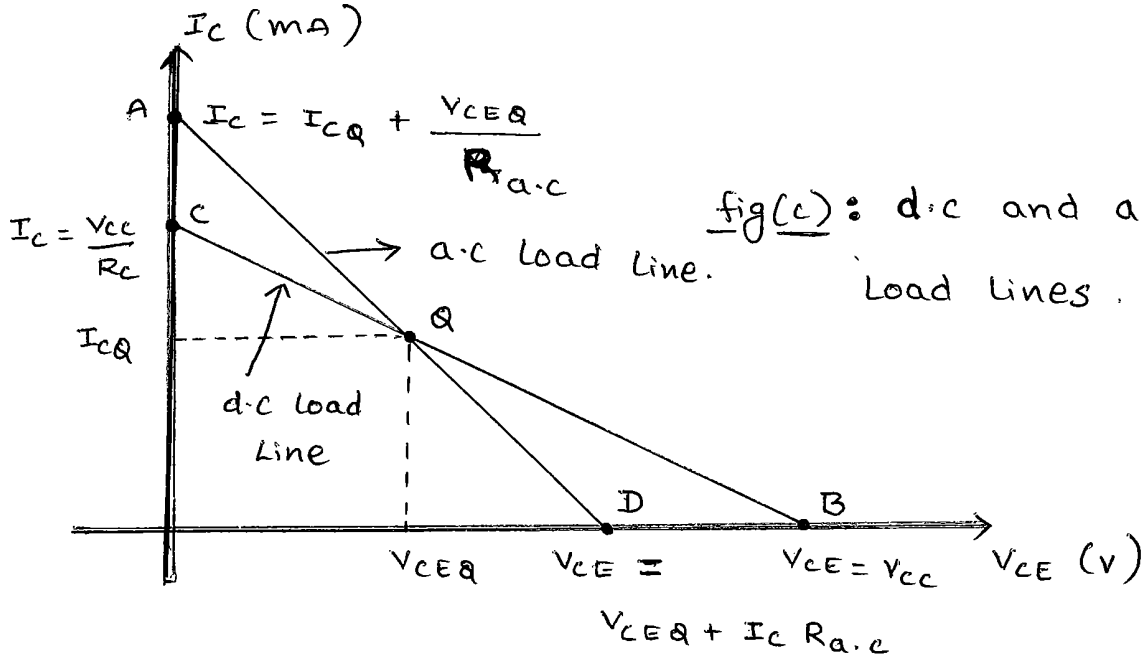
fig(c) shows the ac Equivalent circuit, which is obtained by removing all d.c sources and assming that the capacitors act as short circuit.



After drawing the d.c load line, the operating point Q is properly located at the center of the d.c load line. This operating point is chosen under zero input signal condition of the circuit. Hence a.c load line should also pass through the operating point Q.

The effective a.c load resistance is given by $R_{a.c}$

$$R_{a.c} = R_C \,||\, R_L$$



fig(c): d.c and a.c Load lines.

V_{CEQ} = minimum collector voltage to make the proper transistor biasing

I_{CQ} = minimum collector current to make the proper transistor biasing.

To draw an a.c load line, two end points (ie maximum V_{CE} and maximum I_C) are required

Maximum $V_{CE} = V_{CEQ} + I_{CQ} R_{a.c}$, which locates the point D on the V_{CE} axis.

Maximum $I_C = I_{CQ} + \frac{V_{CEQ}}{R_{a.c}}$, which locates the point C (OC) on the I_C axis.

By joining C and D, a.c load line CD is constructed.

As $R_C > R_{a.c}$, the d.c load line is less steep than the a.c load line.

when the signal is zero, we have the exact d.c conditions.

From the fig(c) it is clear that the intersection of d.c and a.c load line is the operating point 'Q'.

Stabilization :

The maintenance of operating point stable is known as stabilization.

There are two factors which are responsible for shifting the operating point. They are

1) The transistor parameter are temperature dependent.
2) When a transistor is replaced by another of same type, there is a wide spread in the values of transistor parameters.

So, stabilization of the operating point is necessary due to the following reasons.

1) Temperature dependance of I_C
2) Individual Variations and
3) Thermal runaway.

1) Temperature dependence of I_C :

The instability of I_C is principally caused by the following three sources.

i) The ~~ICO~~ I_{CO} doubles for every 10°C rise in temperature.

ii) Increase of β with increase of temperature

iii) The V_{BE} decreases about 2.5mV per °C increase in temperature.

Thermal Runaway :-

2) Individual Variations :-

When a transistor is replaced by another transistor of the same type, the values of β and V_{BE} are not exactly the same. Hence the operating point is changed. So it is necessary to stabilize the operating point irrespective of individual variations in transistor parametens.

3) Thermal runaway :-

Depending upon the construction of a transistor, the collector junction can with-stand maximum temperature. The range of temperature lies between 60°c to 100°c. for 'Ge' transistor and 150°c to 225°c for 'Si' transistor. If the temperature increases beyond this range then the transistor burns out. The increase in the collector junction temperature is due to thermal runaway.

When a collector current flows in a transistor, it is heated ie. its temperature increases. If no stabilization is done, the collector leakage current also increases. This further increases the transistor temperature.

consequently there is a further increase in collector leakage current. The action becomes cumulative and the transistor may ultimately burnout. The self destruction of unstabilized transistor is known as 'thermal runaway'

→ The following two techniques are used for stabilization.

① Stabilization Techniques :-

This technique consists of a biasing circuit which permits a variation of base current I_B, so as to maintain I_C almost constant inspite of variation of I_{CO}, β and V_{BE}.

② Compensation Techniques :-

In this technique, temperature sensitive devices such as diodes, thermistors and sensistors etc are used. Such devices produce compensating voltages and current in such a way that the operating points maintained stable.

→ Stability Factors :-

Since there are three variables which are temperature dependent, we can define three stability factors as below.

1) S : The stability factor 'S' is defined as the rate of change of collector current I_C with respect to the reverse saturation current I_{CO}, keeping β and V_{BE} constant.

$$\text{i.e, } S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}} \Bigg|_{\beta,\ V_{BE} = \text{Constant.}}$$

2) S' : The stability factor S' is defined as the rate of change of I_C with respect to V_{BE} keeping I_{CO} and β constant i.e,

$$S' = \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}} \Bigg|_{\beta,\ I_{CO} \text{ constant.}}$$

3) S'' : The stability factor S'' is defined as the rate of change of I_C with respect to β, keeping I_{CO} and V_{BE} constant i.e,

$$S'' = \frac{\partial I_C}{\partial \beta} = \frac{\Delta I_C}{\Delta \beta} \Bigg|_{V_{BE},\ I_{CO} \text{ Constant.}}$$

Ideally, stability factor should be perfectly zero to keep operating point stable. practically stability factor should have the value as minimum as possible.

Derivation of stability factor :-

For a common emitter configuration collector current is given as

$$I_C = \beta I_B + I_{CEO}$$

$$\Rightarrow I_C = \beta I_B + (1+\beta) I_{CO} \longrightarrow (1)$$

$$[I_{CO} = I_{CBO}]$$

Differentiating equation (1) w.r.t I_C, keeping β constant we get

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta) \frac{\partial I_{CO}}{\partial I_C}$$

$$1 - \beta \frac{\partial I_B}{\partial I_C} = (1+\beta) \frac{\partial I_{CO}}{\partial I_C}$$

$$\Rightarrow \frac{\partial I_C}{\partial I_{CO}} = \frac{(1+\beta)}{1 - \beta \frac{\partial I_B}{\partial I_C}}.$$

$$\Rightarrow S = \frac{1+\beta}{1 - \beta \frac{\partial I_B}{\partial I_C}} \longrightarrow (2)$$

To obtain s' and s'' :

To get s', replace I_B in terms of V_{BE}, in standard equation of I_C.

To get s'', Differentiate equation of I_C w.r.t β, after replacing I_B in terms of V_{BE}.

Methods of Biasing :-

some of the methods used for providing bias for a transistor are as follows.

1) Fixed bias (or) base resistor method.
2) collector to base bias (or) biasing with feedback resistor.
3) voltage divider bias.

1) Fixed bias or Base resistor method :-

A common emitter amplifier using fixed bias circuit is shown in figure below.

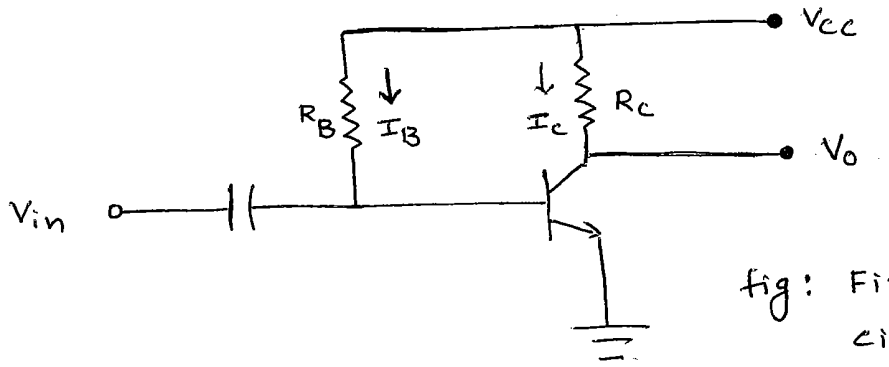


fig: Fixed bias circuit.

In this method, a high resistance R_B is connected between positive terminal of supply V_{cc} and base of the transistor. Here the required zero signal base current flows through R_B and is provided by V_{cc}.

In figure, the base emitter junction is forward biased because the base is positive w.r.t emitter. By a proper selection of R_B,

the required zero signal base current (and hence $I_C = \beta I_B$) can be made to flow.

circuit analysis :-

consider the base-emitter circuit loop of the above figure. (Apply KVL to the base emitter loop)

$$V_{CC} = I_B R_B + V_{BE} \Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

But $I_C = \beta I_B + I_{CEO}$

As I_{CEO} is very small $I_C \simeq \beta I_B$

$$\therefore I_C = \beta \left[\frac{V_{CC} - V_{BE}}{R_B} \right]$$

$\Rightarrow \beta, V_{CC}, V_{BE}$ are constant for a transistor

$\therefore I_C$ depends on R_B

cosider the collector-emitter circuit loop of the circuit. Here apply KVL to the collector ckt then $\boxed{V_{CC} = I_C R_C + V_{CE}}$

stability factor :-

the stability factor S is given by

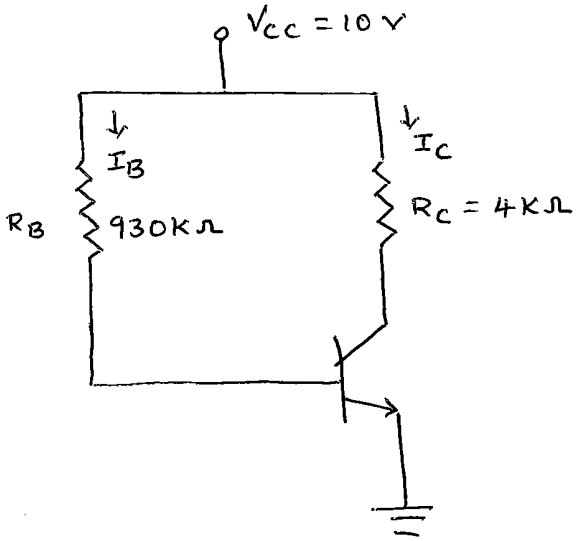
$$S = \frac{1 + \beta}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$

we have $I_B = \frac{V_{CC} - V_{BE}}{R_B}$ = Constant, $\therefore \frac{\partial I_B}{\partial I_C} = 0$

$$\therefore \boxed{S = 1 + \beta}$$

Problem :

Figure below shows a silicon transistor with $\beta = 100$ and biased by fixed bias (or) base resistor method. Determine the operating point.



Solution : Given data

$V_{CC} = 10\,V$, $\beta = 100$, $R_B = 930\,K\Omega$, $R_C = 4K\Omega$, $V_{BE} = 0.7\,V$ (Si transistor)

Applying KVL to the base-emitter loop

$$V_{CC} = I_B R_B + V_{BE}$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10 - 0.7}{930K} = 0.01\,mA$$

$$I_C = \beta I_B = 100 \times 0.01\,mA = 1\,mA.$$

Applying KVL to collector-emitter loop

$$V_{CC} = I_C R_C + V_{CE} \Rightarrow V_{CE} = V_{CC} - I_C R_C$$

$$\Rightarrow V_{CE} = 10 - (1 \times 10^{-3} \times 4 \times 10^{3}) = 6\,V$$

$\therefore$ operating point is $(6V, 1mA)$

Problem :

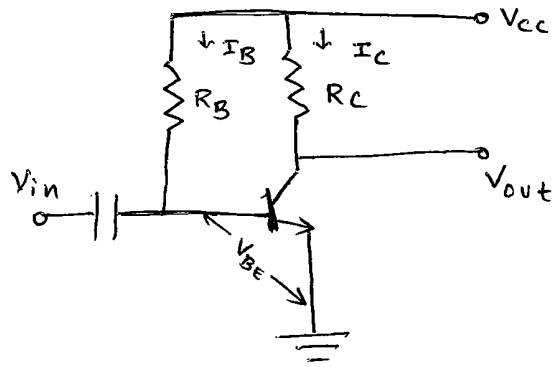
In the fixed bias compensation method shown in figure below, a silicon transistor with $\beta = 100$ is used. $V_{CC} = 6V$, $R_C = 3K\Omega$, $R_B = 530K\Omega$. Draw the dc load line. and determine the operating point. what is the stability factor ?

Solution :- Given data

$\beta = 100$, $V_{CC} = 6V$,

$R_C = 3K\Omega$, $R_B = 530K\Omega$

$V_{BE} = 0.7V$



By applying KVL to the base-emitter loop

$$V_{CC} = I_B R_B + V_{BE}$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{6 - 0.7V}{530K\Omega} = 0.01mA$$

$$\therefore I_C = \beta I_B = 0.01m \times 100 = 1mA$$

$$\therefore \boxed{I_C = 1mA}$$

Applying KVL to the collector-emitter loop

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C = 6 - (1m \times 3k)$$

$$\therefore \boxed{V_{CE} = 3V}$$

$\therefore$ operating point = $(3V, 1mA)$

Stability factor $S = \beta + 1 = 100 + 1 = 101$

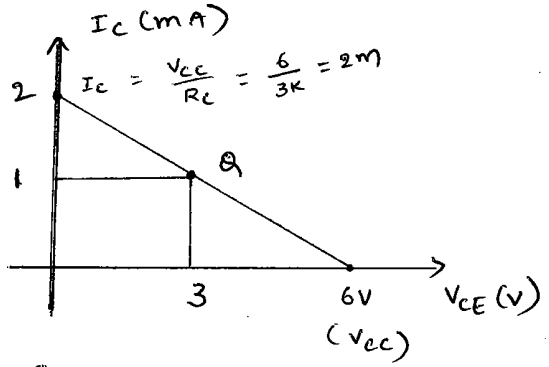


fig : DC Load line.

Advantages of Fixed bias circuit :-

1. This is a simple circuit which uses very few components.
2. The operating point can be fixed anywhere in the active region of the characteristics simply changing the values of R_B. Thus it provides maximum flexibility in the design.

Disadvantages of Fixed bias circuit :

1. With the rise in temperature the operating point is not stable.
2. When the transistor is replaced by another with the different value of β, the operating point will shift ie: the stabilization of operating point is very poor in fixed bias circuit.

Because of these disadvantages, the fixed bias circuit require some modifications. In the modified circuit, R_B is connected between collector and base. Hence the circuit is called "collector to base bias" circuit.

Collector to Base bias (or) Biasing with feedback resistor :

A common emitter amplifier using collector to base bias circuit is shown in figure below. This circuit is the simplest way to provide some degree of stabilisation to the amplifier operating point.

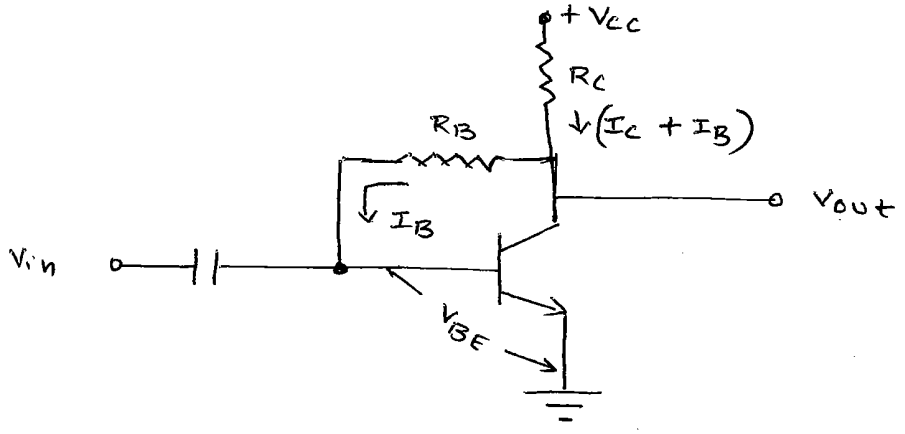


fig: collector to base circuit.

If the collector current I_C tends to increase due to either increase in temperature or the transistor has been replaced by the one with a higher β, the voltage drop across R_C increases, thereby reducing the value of V_{CE}. Therefore I_B decreases which in turn compensates the increase in I_C. Thus greater stability is obtained.

Circuit Analysis :-

Consider the base-emitter circuit, applying the KVL to the circuit, we get

$$V_{CC} = (I_C + I_B) R_L + I_B R_B + V_{BE}$$

$$V_{CC} = I_B (R_C + R_B) + I_C R_C + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B}$$

But $I_C = \beta I_B \Rightarrow I_C = \frac{\beta (V_{CC} - V_{BE} - I_C R_C)}{R_C + R_B}$

Consider the collector - emitter circuit, applying the KVL to the circuit, we get.

$$V_{CC} = (I_B + I_C) R_C + V_{CE}.$$

$$V_{CE} = V_{CC} - (I_C + I_B) R_C.$$

Stability factor 'S' :-

The stability factor S is given by

$$S = \frac{1 + \beta}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$

we have $I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C}$ = Constant

differentiating the above equation w.r.t I_C we get

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_B + R_C}$$

$$\therefore S = \frac{1 + \beta}{1 + \beta \left(\frac{R_C}{R_B + R_C} \right)}$$

The stability factor S is smaller than the value obtained by fixed bias circuit. Also 'S' can be made smaller by making R_B small (or) R_C large.

Problem :-

In the biasing with feedback resistor method, a silicon transistor with feedback resistor is used. The operating point is at 7V, 1mA and $V_{CC} = 12V$, Assume $\beta = 100$, Determine

a) the value of R_B

b) stability factor

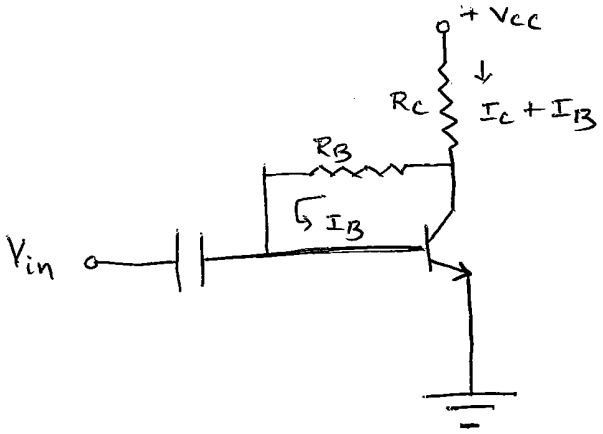
c) what will be the new operating point if $\beta = 50$ with all other circuit values are same.

Solution : Here for Si transistor $V_{BE} = 0.7V$

a) To determine R_B :

The operating point is at $V_{CE} = 7V$ and $I_C = 1mA$

$$I_C = \beta I_B \Rightarrow I_B = \frac{I_C}{\beta} = \frac{1mA}{100} = 10\mu A.$$



$$R_C = \frac{V_{CC} - V_{CE}}{I_C + I_B} = \frac{12 - 7}{1 \times 10^{-3}} = 5\ k\Omega$$

(I_B is negligible)

$$R_B = \frac{V_{CC} - V_{BE} - I_C R_C}{I_B} = \frac{12 - 0.7 - (1 \times 10^{-3} \times 5 \times 10^3)}{10 \times 10^{-6}}$$

$$R_B = 630\ k\Omega.$$

b) stability factor $S = \dfrac{1 + \beta}{1 + \beta \left(\dfrac{R_C}{R_C + R_B} \right)} = 56.5$

c) To determine new operating point when $\beta = 50$

$$V_{CC} = (I_B + I_C) R_C + I_B R_B + V_{BE}$$

$$V_{CC} = (I_B + \beta I_B) R_C + I_B R_B + V_{BE}$$

$$V_{CC} - V_{BE} = I_B (R_C + \beta R_C + R_B)$$

$R_C = 5\ K\Omega$, $R_B = 630\ K\Omega$, $V_{CC} = 12\ V$, $V_{BE} = 0.7$

$\therefore I_B = 12.84\ \mu A.$

$\therefore I_C = \beta I_B = 50 \times 12.84 \times 10^{-6} = 0.64\ mA$

Apply KVL to the collector ckt

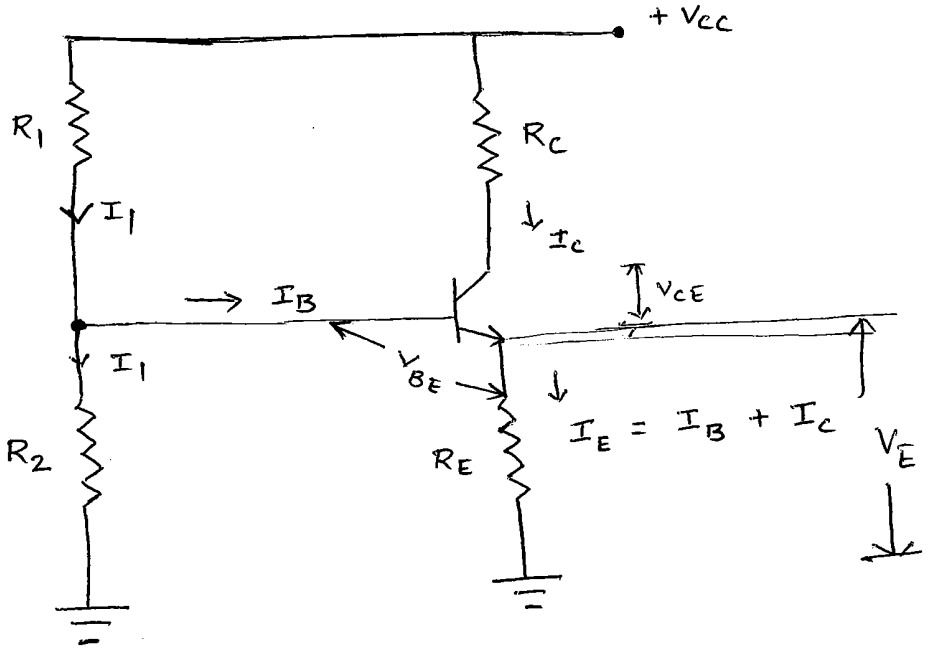
$$V_{CC} = (I_B + I_C) R_C + V_{CE}$$

$\Rightarrow V_{CE} = 8.79\ V.$

$\therefore$ New operating point = (8.79 V, 0.64 mA)

Voltage divider bias (or) self bias (or) Emitter bias :-

A simple circuit used to establish a stable operating point is the self bias configuration. This self bias ckt is also called Emitter bias or voltage divider bias circuit, that can be used for low collector resistance is shown in figure below.



The current in the emitter resistor R_E causes a voltage drop which is in the direction to reverse bias the emitter junction. For the transistor to remain in the active region, the base emitter junction has to be forward biased. the required base bias is obtained from the power supply through the voltage divider network of the resistances R_1 and R_2.

Circuit analysis :-

Suppose that the current flowing through resistance R_1 is I_1. As base current I_B is very small, the current flowing through R_2 can also be taken as I_1.

(i) Collector current I_C :

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

Voltage across resistance R_2,

$$V_2 = V_{CC} \cdot \frac{R_2}{R_1 + R_2}$$

Applying Kirchoff's voltage law to the base circuit

$$V_2 = V_{BE} + V_E$$

$$V_2 = V_{BE} + I_E R_E$$

$$I_E = \frac{V_2 - V_{BE}}{R_E}$$

$$I_C = \frac{V_2 - V_{BE}}{R_E} \qquad \left[\because I_E \simeq I_C \right] \longrightarrow (1)$$

It is clear from expression (1) that I_C does not at all depend upon β. Though I_C depends upon V_{BE}, but $V_2 >> V_{BE}$, so that I_C is practically independent of V_{BE}. Thus I_C in this circuit is almost independent of transistor parametens and hence good stabilisation is ensured.

(ii) collector - emitter voltage (V_{CE}) :-

Applying Kirchoff's voltage law to the collector side

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$V_{CC} = I_C (R_C + R_E) + V_{CE} \quad \left[\because I_E \simeq I_C \right]$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Stabilisation : Excellent stabilisation is provided by R_E. Consideration of eq ① reveals this fact

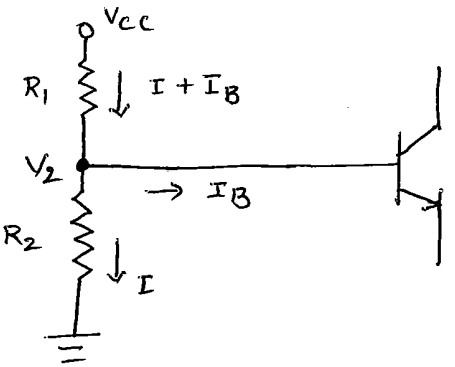
$$I_C = \frac{V_2 - V_{BE}}{R_E}$$

$$V_2 = V_{BE} + I_C R_E$$

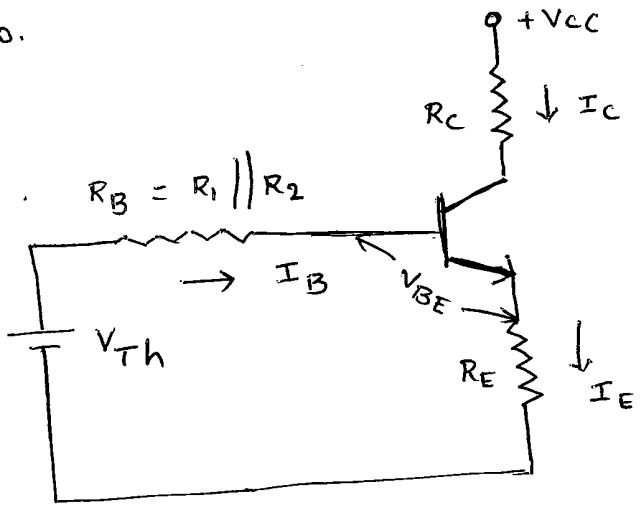
Suppose the collector current I_C increases due to rise in temperature. This will cause the voltage drop across the emitter resistance R_E to increase ($I_E R_E \simeq I_C R_E$ increases). As voltage drop across R_2 (ie V_2) is independent of I_C, therefore V_{BE} decreases. This inturn causes I_B to decrease. The reduced value of I_B tends to restore I_C to the original value.

Stability factor :-

The thevinin equivalent circuit of voltage - divider bias is as shown below.



the simplified equivalent circuit is shown in figure below.



From above figures $V_2 = V_{Th} = V_{cc}\left(\frac{R_2}{R_1+R_2}\right)$

$$R_{th} = R_B = R_1 \,||\, R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Applying KVL to the base circuit

$$V_{Th} = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

Differentiating w.r.t I_C and considering V_{BE} to be independent of I_C we get

$$0 = \frac{\partial I_B}{\partial I_C} \times R_B + \frac{\partial I_B}{\partial I_C} R_E + R_E$$

$$\frac{\partial I_B}{\partial I_C}\left(R_E + R_B\right) = -R_E$$

$$\therefore \quad \frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_E + R_B}$$

The generalized expression for stability factor 's' is given by $S = \dfrac{1+\beta}{1-\beta\dfrac{\partial I_B}{\partial I_C}}$.

substituting the value of $\frac{\partial I_B}{\partial I_C}$ in the above equation, we get

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E+R_B}\right)}$$

$$S = \frac{(1+\beta)(R_E+R_B)}{R_B+R_E+\beta R_E} = \frac{(1+\beta)(R_E+R_B)}{R_B+(1+\beta)R_E}$$

Dividing N.M and D.M by R_E we get

$$S = (1+\beta)\left(\frac{1+\frac{R_B}{R_E}}{(1+\beta)+\frac{R_B}{R_E}}\right)$$

The ratio $\frac{R_B}{R_E}$ controls the value of stability factor 'S'.

If $\frac{R_B}{R_E} << 1$ then above equation reduces to

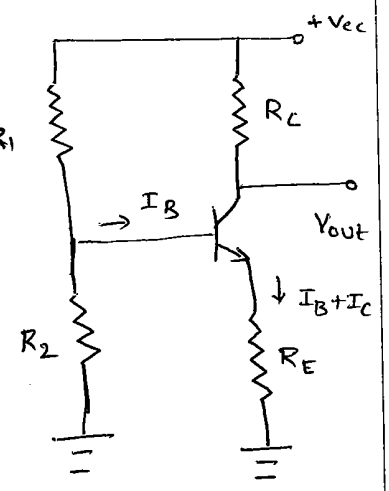
$$S = (1+\beta)\cdot\left(\frac{1}{1+\beta}\right) = 1$$

Practically $\frac{R_B}{R_E} \neq 0$, but to have better stability factor 'S', we have to keep $\frac{R_B}{R_E}$ as small as possible.

Stability factor 's' for voltage divider bias (or) self bias is less as compared to other biasing circuits. so this circuit is most commonly used.

Problem:

In a CE germanium transistor amplifier circuit, the bias is provided by self bias shown in figure. The various parameters are $V_{CC} = 16V$, $R_C = 3K\Omega$, $R_E = 2K\Omega$, $R_1 = 56K\Omega$, $R_2 = 20K\Omega$ and $\alpha = 0.985$.



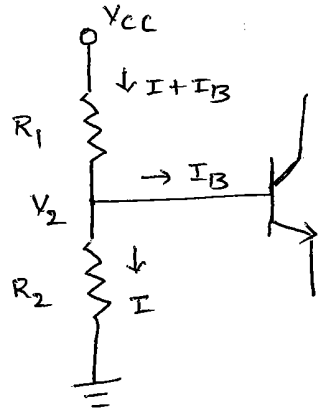
Determine a) the co-ordinates of the operating point.
and b) the stability factor S.

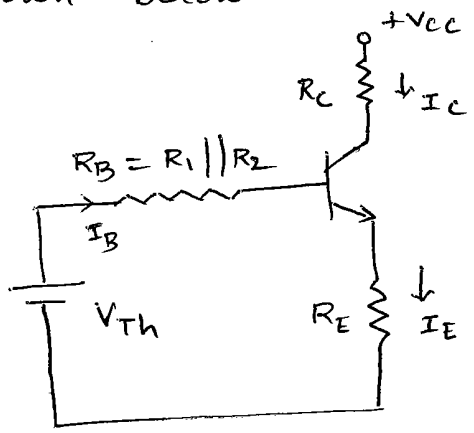
Solution: For a Ge transistor $V_{BE} = 0.3\ V$

As $\alpha = 0.985$, $\beta = \frac{\alpha}{1-\alpha} = \frac{0.985}{1-0.985} = 66$

a) To find the co-ordinates of the operating Point:-

The thevinins equivalent circuits of voltage divider bias circuits is as shown below.





Thevinins voltage $V_2 = V_{Th} = \frac{R_2}{R_1+R_2} \cdot V_{CC}$

Substituting all the values $V_{Th} = 4.21\ V$.

Thevinins resistance $R_B = \frac{R_1 R_2}{R_1 + R_2} = 14.737\ K\Omega$.

The loop equation around the base circuit is

$$V_{Th} = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$V_{Th} = \frac{I_C}{\beta} R_B + V_{BE} + \left(\frac{I_C}{\beta} + I_C \right) R_E$$

Substituting all the values $I_C = 1.73\ mA$.

Since I_B is very small $I_C \simeq I_E = 1.73\ mA$.

$$\therefore \quad V_{CC} = V_{CE} + I_C R_C + I_E R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$\therefore \quad V_{CE} = 7.35\ V.$$

$\therefore$ operating point $= (V_{CE}, I_C) = (7.35V, 4.7K\Omega)$

(b) $S = (1+\beta)\left(\frac{1 + \frac{R_B}{R_E}}{1 + \beta + \frac{R_B}{R_E}}\right) = 7.537.$

Bias Compensation :-

The biasing circuits provide stability of operating point in case of variations in the transistor parametens such as I_{CO}, V_{BE} and β.

The stabilization techniques refer to the use of resistive biasing circuits which permit I_B to vary so as to keep I_C relatively constant.

on the other hand, compensation techniques refer to the use of temperature sensitive devices such as diodes, thermistons and sensistons ~~can~~ etc, to compensate for the

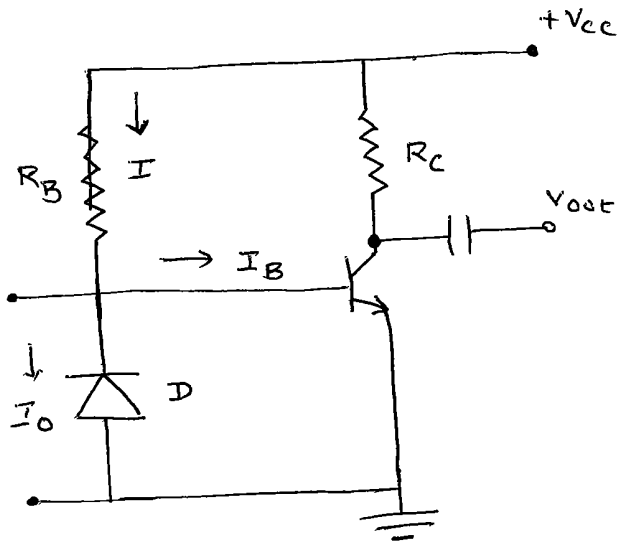
Variation in currents. Sometimes for excellent bias and thermal stabilization, both stabilization as well as compensation techniques are used.

The following are some compensation techniques

1) Diode compensation
2) Thermistor compensation
3) Sensistor compensation.

1) Diode Compensation :-

Figure shows a transistor amplifier with a Diode D connected across the base emitter junction for compensation of change in collector saturation current I_{CO}.



The diode is of the same material as the transistor and it is reverse biased by the base emitter junction voltage V_{BE}, allowing the diode reverse saturation current I_o to flow through diode (D). The base current $I_B = I - I_o$.

As long as temperature is constant, diode D operates as a resistor. As the temperature increases, I_{CO} of the transistor increases. Hence, to compensate for this the base current I_B should be decreased.

The increase in temperature will also cause the Leakage current I_o through D to increase and thereby decreasing the base current I_B. This is the required action to keep I_C constant.

(2) Thermistor compensation :-

In this figure, a thermistor R_T, having a negative temperature coefficient is connected, in parallel with R_2.

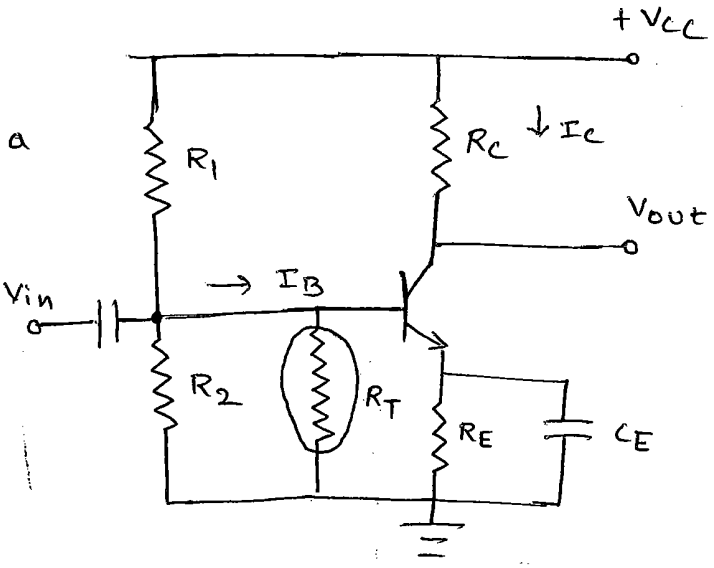


Fig: Thermistor bias compensation

The resistance of thermistor decreases exponentially with increase of temperature. An increase in temperature will decrease the base voltage V_{BE}, reducing I_B and I_C. Bias stabilization is also provided by R_E and C_E.

(3) Sensistor compensation :-

In the figure shown below, a sensistor R_s having a positive temperature co-efficient is connected across R_1 (or R_c). R_s increases

with temperature. As temperature increases the equivalent resistance of the parallel combination of R_1 and R_S also increases. and hence the base voltage V_{BE} decreases, reducing I_B and I_C. This reduced I_C compensates for the increased I_C caused by the increase in I_{CO}, V_{BE} and β due to temperature rise.

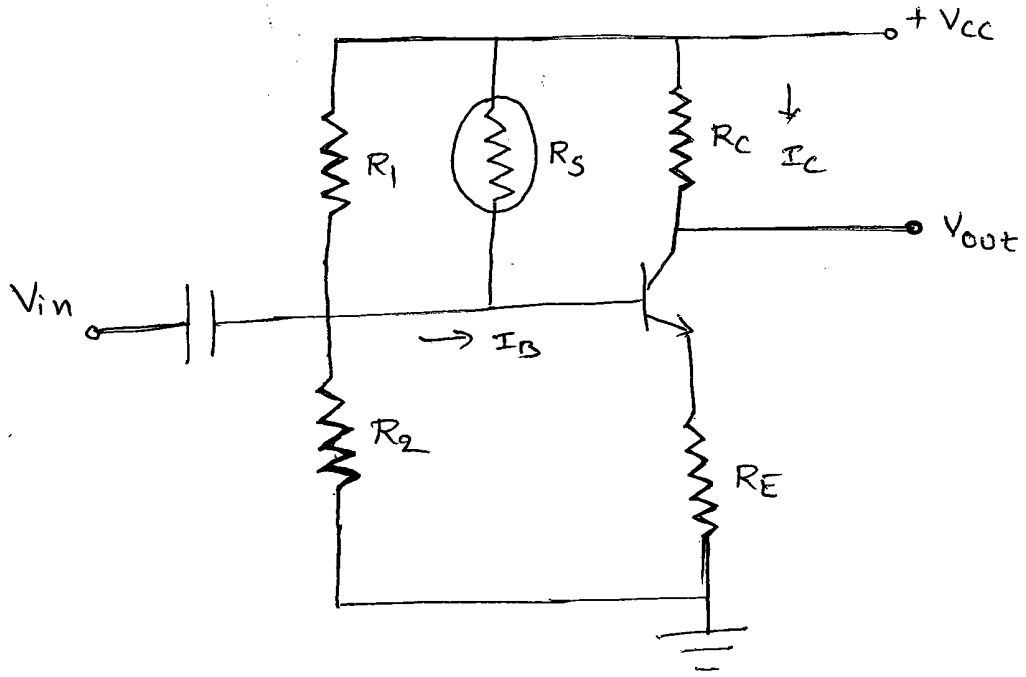


Fig: Sensistor bias Compensation.